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59. <<DC JACK IN IO BD>>
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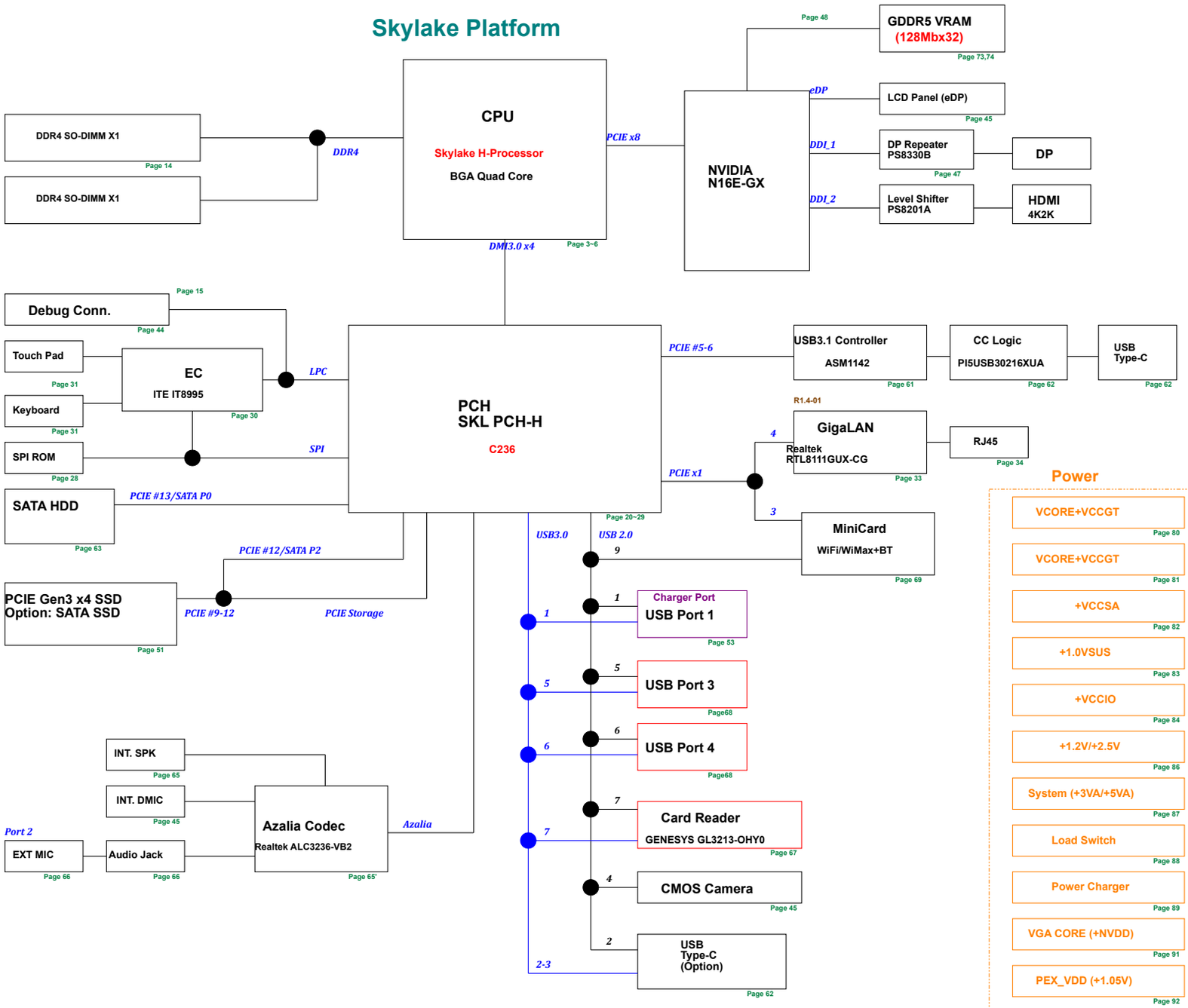
GL502VM Block Diagram

Skylake Platform



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Project Name	GL502	Rev	1.0
Title :	Block Diagram		
Size	Custom	Dept.:	ASUSTeK COMPUTER INC.
Engineer:	RD1_EE1		
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PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	NC(H)	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_EBCHIP_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWARN#	Native	ME_BusPwrDnAck		PU 10K(E)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16			
GPP_A17	GPI	GPI	(N.C)			
GPP_A18	GPI	GPI	(N.C)			
GPP_A19	GPI	GPI	(N.C)			
GPP_A20	GPI	GPI	(N.C)			
GPP_A21	GPI	GPI	(N.C)			
GPP_A22	GPI	GPI	(N.C)			
GPP_A23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPO	GPO	(N.C)			
GPP_B2	GPI	GPI	(N.C)			
GPP_B3	GPI	GPI	(N.C)			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_FREQ_REQ0#		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLKREQ3_WLAN#_X1		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLKREQ4_CLAMP_X1		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLKREQ5_TBT#_X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MSWY_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPP914	PD		
GPP_B15	GPI	Native	GSPI0_CS#			
GPP_B16	GPI	Native	GSPI0_CLK			
GPP_B17	GPI	Native	GSPI0_MISO			
GPP_B18	GPO	Strap	PCH_GPP918	PD		
GPP_B19	GPI	GPO	PCH_GPP919/WT_ON_PCH		PD 10K(E)	
GPP_B20	GPI	GPO	PCH_GPP920/GPUEVENT#_PCH		PU 10K(E)	+3VSUS
GPP_B21	GPI	GPI	PCH_GPP921/GC6FB#_PCH		PU 10K(E)	+3VS
GPP_B22	GPO	Strap	PCH_GPP922	PD		
GPP_B23	GPO	GPO	SMILABERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPI	Strap	PCH_GPPC2			
GPP_C3	SMLOCLK	Native	SMLO_CLK		PU 2.2K	+3VSUS
GPP_C4	SMLODATA	Native	SMLO_DAT		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		+3VSUS
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPI	PCH_GPPC8			
GPP_C9	GPI	GPI	PCH_GPPC9			
GPP_C10	GPI	GPI	PCH_GPPC10			
GPP_C11	GPI	GPI	PCH_GPPC11			
GPP_C12	GPI	GPI	DIMM_SELO		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NFC_ID		PD 10K	+3VSUS
GPP_C16	GPI	GPO	AOAC_WLANLED		PU 10K(E)	+3VSUS
GPP_C17	GPI	GPO	PCH_GPPC17		PU 10K(E)	+3VS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PD 10K(E)	
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	PCH_GPPC22/DGPU_PWR_EN#		PD 10K(E)	+3VSUS
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	CIO_PLUG_EVENT			
GPP_D1	GPO	GPO	GPIO_3_PCHPE_PWR			
GPP_D2	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_D3	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_D4	GPI	GPI	(N.C)			
GPP_D5	GPI	GPI	(N.C)			
GPP_D6	GPI	GPI	(N.C)			
GPP_D7	GPI	GPO	WLAN_ON#		PD 100K(E)	
GPP_D8	GPI	GPI	(N.C)			
GPP_D9	GPI	Strap	PCH_ID0		PD 10K	
GPP_D10	GPI	Strap	PCH_ID1		PD 10K	
GPP_D11	GPI	Strap	TOUCHPAD_ID		PD 10K(E)	
GPP_D12	GPI	Strap	TOUCH_PANEL_ID		PD 10K(E)	
GPP_D13	GPI	GPI	PCH_GPP_D13		PU 10K(E)	+3VSUS
GPP_D14	GPO	GPO	PCH_GPP_D14/WLAN_LED		PD 100K	
GPP_D15	GPO	GPO	PCH_GPP_D15/WLAN_BT_LED		PD 100K	
GPP_D16	GPI	GPI	(N.C)			
GPP_D17	GPI	GPI	(N.C)			
GPP_D18	GPI	GPI	(N.C)			
GPP_D19	GPI	GPI	(N.C)			
GPP_D20	GPI	GPI	(N.C)			
GPP_D21	GPI	GPO	LED_Record			
GPP_D22	GPI	GPI	(N.C)			
GPP_D23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	GPI	SATAPCIE_DET0		PU 10K	+3VS
GPP_E1	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E3	GPI	GPI	(N.C)		PU 10K(E)	+3V
GPP_E4	GPI	Native	MOFFO_DEVSLP		PU 10K(E)	+3VS
GPP_E5	GPI	Native	SATA1_DEVSLP		PU 10K(E)	+3VS
GPP_E6	GPI	Native	MOFF1_DEVSLP			
GPP_E7	GPI	GPI	(N.C)			
GPP_E8	GPI	Native	SATA_LED#		PU 10K(E)	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPI	(N.C)			
GPP_F1	GPI	GPO	(N.C)			
GPP_F2	GPI	GPI	(N.C)			
GPP_F3	GPI	GPI	(N.C)			
GPP_F4	GPI	GPI	(N.C)			
GPP_F5	GPI	Native	SATA1_HDD_DEVSLP		PU 10K(E)	+3VS
GPP_F6	GPI	Native	(N.C)			
GPP_F7	GPI	GPI	(N.C)			
GPP_F8	GPI	GPI	(N.C)			
GPP_F9	GPI	GPI	(N.C)			
GPP_F10	GPI	GPI	(N.C)			
GPP_F11	GPI	GPI	(N.C)			
GPP_F12	GPI	GPI	(N.C)			
GPP_F13	GPI	GPI	(N.C)			
GPP_F14	GPI	GPI	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	GPI	(N.C)		(N.C)	
GPP_F20	GPI	GPI	(N.C)			
GPP_F21	GPI	GPI	(N.C)		(N.C)	
GPP_F22	GPI	GPI	(N.C)			
GPP_F23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPI	(N.C)			
GPP_G1	GPI	GPO	(N.C)			
GPP_G2	GPI	GPI	(N.C)			
GPP_G3	GPI	GPI	(N.C)			
GPP_G4	GPI	GPI	(N.C)			
GPP_G5	GPI	GPI	(N.C)			
GPP_G6	GPI	GPI	(N.C)			
GPP_G7	GPI	GPI	(N.C)			
GPP_G8	FAN_PWM_0	Native	(N.C)			
GPP_G9	FAN_PWM_1	Native	(N.C)			
GPP_G10	FAN_PWM_2	Native	(N.C)			
GPP_G11	FAN_PWM_3	Native	(N.C)			
GPP_G12	GPI	GPI	(N.C)			
GPP_G13	GPI	GPI	(N.C)			
GPP_G14	GPI	GPI	(N.C)			
GPP_G15	GPI	GPI	(N.C)			
GPP_G16	GPI	GPI	(N.C)			
GPP_G17	GPI	GPI	(N.C)			
GPP_G18	GPI	GPI	PCH_GPP_G18			
GPP_G19	GPI	GPI	PCH_GPP_G19			
GPP_G20	GPI	GPI	(N.C)			
GPP_G21	GPI	GPI	(N.C)			
GPP_G22	GPI	GPI	(N.C)			
GPP_G23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ6_NGFF1#_X1		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H5	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H6	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H7	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H8	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H9	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	(N.C)		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	(N.C)			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPI	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	(N.C)			
GPP_H21	GPI	GPI	(N.C)			
GPP_H22	GPI	GPI	(N.C)			
GPP_H23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPI	(N.C)		(N.C)	
GPP_I1	GPI	GPI	(N.C)		(N.C)	
GPP_I2	GPI	GPI	(N.C)			
GPP_I3	GPI	GPI	(N.C)			
GPP_I4	GPI	GPI	GPP_I4		PU 100K	
GPP_I5	GPI	GPI	(N.C)		(N.C)	(N.C)
GPP_I6	GPO	GPO	(N.C)	(N.C)	(N.C)	(N.C)
GPP_I7	GPI	GPI	(N.C)		(N.C)	(N.C)
GPP_I8	GPO	GPO	(N.C)	(N.C)	(N.C)	(N.C)
GPP_I9	GPI	GPI	(N.C)		(N.C)	(N.C)
GPP_I10	GPO	GPO	(N.C)	(N.C)	(N.C)	(N.C)

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	PCH_GPD2#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(E)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUS3#		PD 150K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUS5#		PD 150K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	PWROK	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(E)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PWREN		PU 10K	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	(N.C)	
GPA1	OD	GPO	CHG_LED#	PU 10K (E)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (E)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN2_PWM		
GPA6	Alt	PWM	PM_LED_PWM		
GPA7	O	GPO	GS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_EC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PX_EN_EC		
GPB5	O	GPO	HKey_WAKE	PD 10K	
GPB6	OD	GPO	BC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (E)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_THRMTRIP#	PU 10K (E)	+3VSUS
GPC4	I	GPI	EC_SATA/CHP1#	PU 10K (E)	+3VSUS
GPC5	I	GPI	PM_SUSC#	PU 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU 100K	
GPC7	O	GPO	EC_SPC7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_SUS#		
GPD1	O	GPO	EC_GPD1/WAC_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/LOW_SIX#		
GPD6	Alt	GPI	FAN2_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PU 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PU 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	SUSWARN# _VCC		
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUS6#	PU 100K	
GPE6	OD	GPO	EC_GPE6		
GPE7	OD	GPO	THRO_CPU#	PU 10K(E) (N.C)	+3VA_EC (N.C)

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0 CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0 DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PHOLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCK#/EC_SCK#_PCH	PU 10K (E)	
GPG4	GPI		EC_SI/EC_SI_PCH	PU 10K (E)	
GPG5	GPI		EC_SO/EC_SO_PCH	PU 10K (E)	
GPG6	O	GPO	USB30_5VSUS		
GPG7	GPI		EC_SCK_PCH	PU 10K (E)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB1 CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB1 DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_SUSC#_PCH	PU 10K (E)	
GPH4	O	GPO	DPWROK_EC	PU 10K	
GPH5	O	GPO	PM_PWROK	PU 10K	
GPH6	O	GPO	PM_SYSPWROK	PU 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_S0IX#		
GPI1	I	GPI	SYSSUS_PWRGD		
GPI2	I	GPI	ALL_SYSPWR_PWRGD	(N.C)	(N.C)
GPI3	I	GPI	IMVP9_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	(N.C)	(N.C)
GPI7	Alt	AD	WA_MAX_POWER	PU 100K & PD 56K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB11_5VSUS#	PU 10K	+3VSUS
GPJ1	O	GPO	3VAOSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	PL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	EC_GPJ6/EC_WAKE#	PU 100K(E)	+3VA_DSW
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/ECI0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/ECO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/ECO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/ECC3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/EDCK		CLK_EBCHIP1_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

N501VW Setting

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
on board memory CHA	
SO-DIMM B(0)	A4h

EC Master (SMB1)	SM-Bus Address
SM-Bus Device	
VGA Thermal Sensor	90h
CPU Thermal Sensor	98h
Power Thermal Sensor	70h

Device Identification

CPU Thermal Sensor	
1st	0x4d/211d/M
2nd	

GL502VW PCIE & USB Function define

Skylake HM170

XUD	XDD Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3_IO	
02	USB3#02 / SSIC#01		
03	USB3#03 / SSIC#02		
04	USB3#04		
05	USB3#05	USB3_IO	
06	USB3#06	USB3_IO	
07	USB3#07 / PCIE#01	CardReader, USB3(RSV)	SRC1
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	GLAN	SRC4
11	PCIE#05 / GBE		SRC5
12	PCIE#06	TBT	
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE		
16	PCIE#10 / SATA#1	PCIE*4 SSD	SRC6
17	PCIE#11	SATA SSD	
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3	1st HDD	
23			
24			
25			
26			

USB 2.0	Function
USB2_01	USB3.0 MB Port1
USB2_02	
USB2_03	
USB2_04	Camera
USB2_05	USB3.0 IO Port1
USB2_06	USB3.0 IO Port2
USB2_07	CardReader
USB2_08	N-Key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

SKL PCH-H Z170 HSIO

1	USB3 #1 (OTG)				
2	USB3 #2	SSIC #1			
3	USB3 #3	SSIC #2			
4	USB3 #4				
5	USB3 #5				
6	USB3 #6				
7	USB3 #7	PCIE #1	x2	x4	NA
8	USB3 #8	PCIE #2	x2		
9	USB3 #9	PCIE #3	x2	x4	NA
10	USB3 #10	PCIE #4	GbE		
11	PCIE #5		GbE	x2	
12	PCIE #6			x2	
13	PCIE #7			x2	
14	PCIE #8			x2	
15	PCIE #9	SATA #0	GbE	x2	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1		x2	
17	PCIE #11			x2	
18	PCIE #12		GbE	x2	
19	PCIE #13	SATA #0*	GbE	x2	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*		x2	
21	PCIE #15	SATA #2		x2	
22	PCIE #16	SATA #3		x2	
23	PCIE #17	SATA #4		x2	Intel IRST PCIE Storage Device #3
24	PCIE #18	SATA #5		x2	
25	PCIE #19	SATA #6		x2	
26	PCIE #20	SATA #7		x2	

SKL PCH-H H170 HSIO

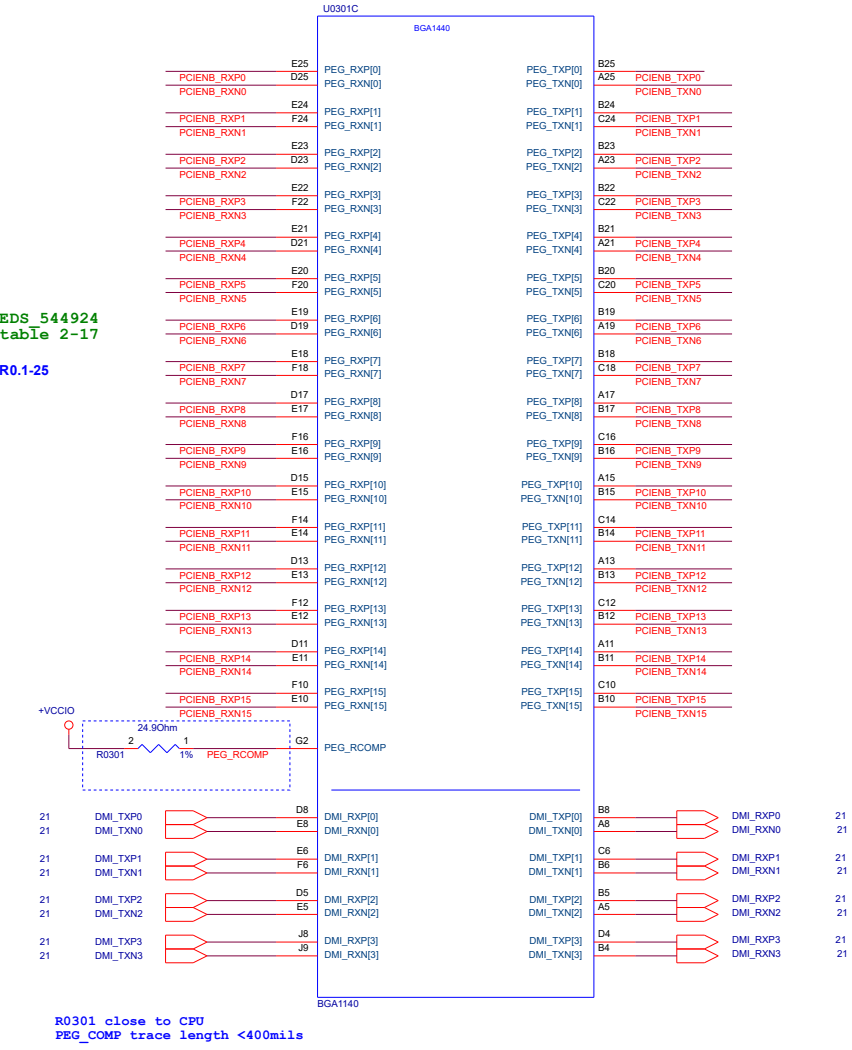
1	USB3 #1 (OTG)				
2	USB3 #2	SSIC #1			
3	USB3 #3	SSIC #2			
4	USB3 #4				
5	USB3 #5				
6	USB3 #6				
7	USB3 #7				
8	USB3 #8				
9	PCIE #3			x2	NA
10	PCIE #4		GbE		
11	PCIE #5		GbE	x2	NA
12	PCIE #6			x2	
13	PCIE #7			x2	
14	PCIE #8			x2	
15	PCIE #9	SATA #0	GbE	x2	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1		x2	
17	PCIE #11			x2	
18	PCIE #12		GbE	x2	
19	PCIE #13	SATA #0*	GbE	x2	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*		x2	
21	PCIE #15	SATA #2		x2	
22	PCIE #16	SATA #3		x2	
23	SATA #4			NA	NA
24	SATA #5				
25	PCIE #19			NA	
26	PCIE #20				

SKL PCH-H HM170 HSIO

1	USB3 #1 (OTG)				
2	USB3 #2	SSIC #1			
3	USB3 #3	SSIC #2			
4	USB3 #4				
5	USB3 #5				
6	USB3 #6				
7	USB3 #7	PCIE #1	x2	x4	NA
8	USB3 #8	PCIE #2	x2		
9	PCIE #3		x2	x4	NA
10	PCIE #4		GbE		
11	PCIE #5		GbE	x2	
12	PCIE #6			x2	
13	PCIE #7			x2	
14	PCIE #8			x2	
15	PCIE #9	SATA #0	GbE	x2	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1		x2	
17	PCIE #11			x2	
18	PCIE #12		GbE	x2	
19	PCIE #13	SATA #0*	GbE	x2	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*		x2	
21	PCIE #15	SATA #2		x2	
22	PCIE #16	SATA #3		x2	
23				NA	NA
24					
25				NA	
26					

ASUS	Project Name: GL502		Rev: 1.0
Title: System Setting			
Size: B	Project code: 90NR0DA1-M0XXX0	Engineer: RD1_EE1	
Date: Monday, July 06, 2015	Sheet 2 of 50		

PCIEG

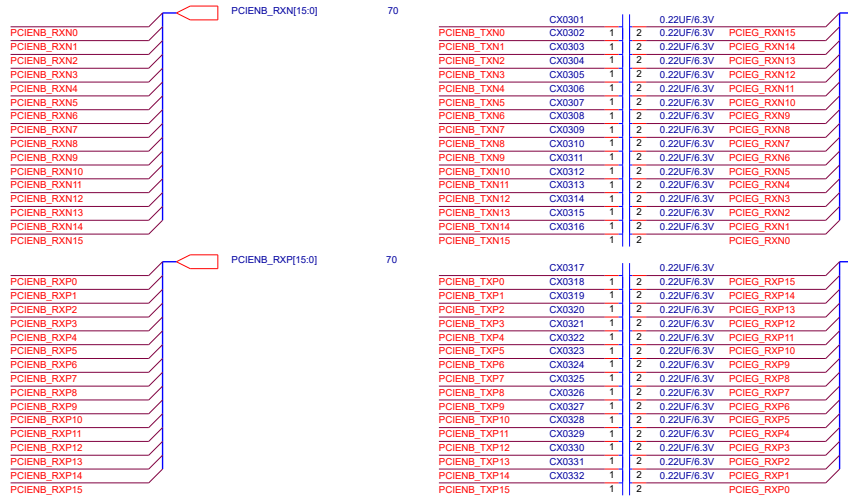


EDS_544924
table 2-17

R0.1-25

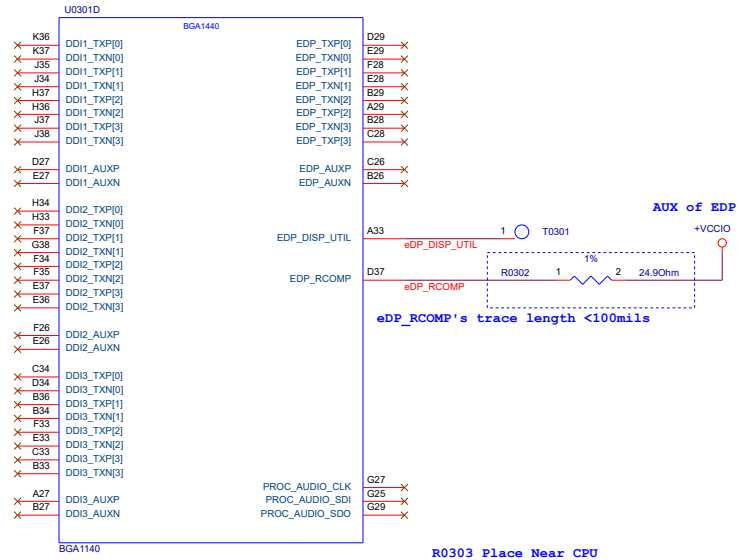
R0301 close to CPU
PEG_COMP trace length <400mils

PCIENB_RXN[15:0] 70
PCIENB_RXP[15:0] 70



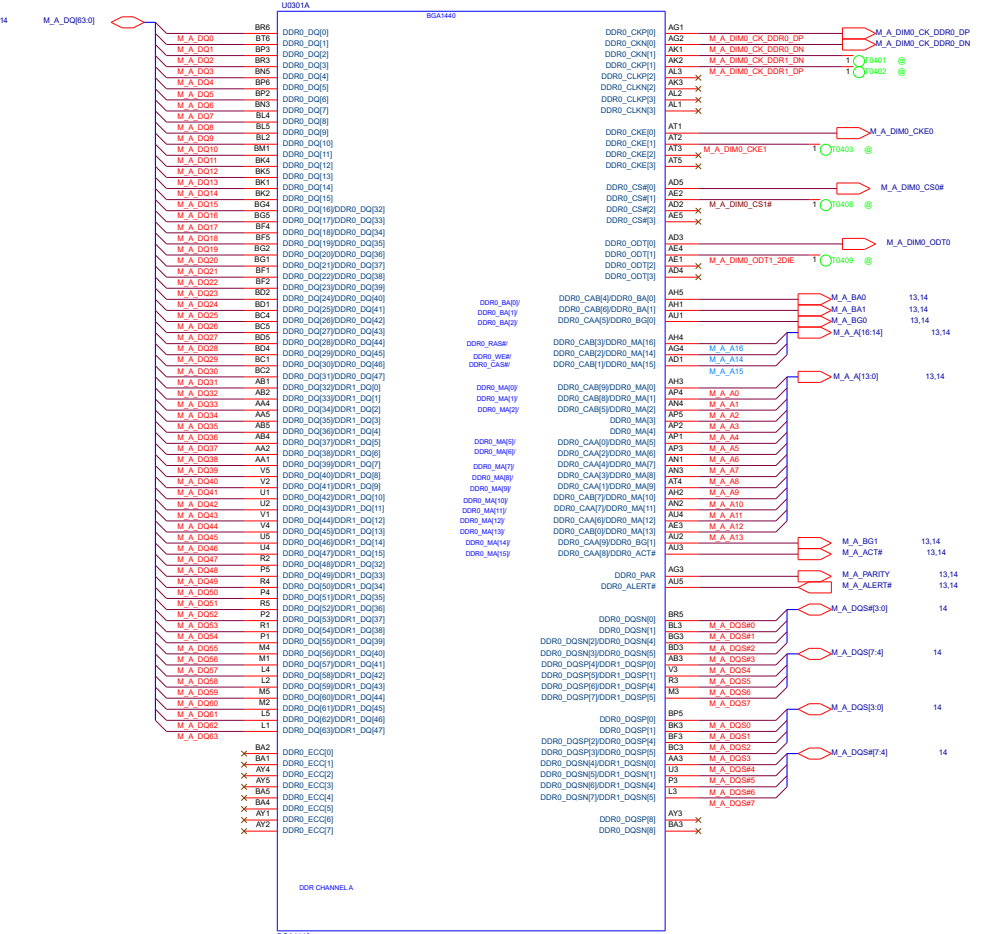
PCIEG_RXN[15:0] 70
PCIEG_RXP[15:0] 70

Display

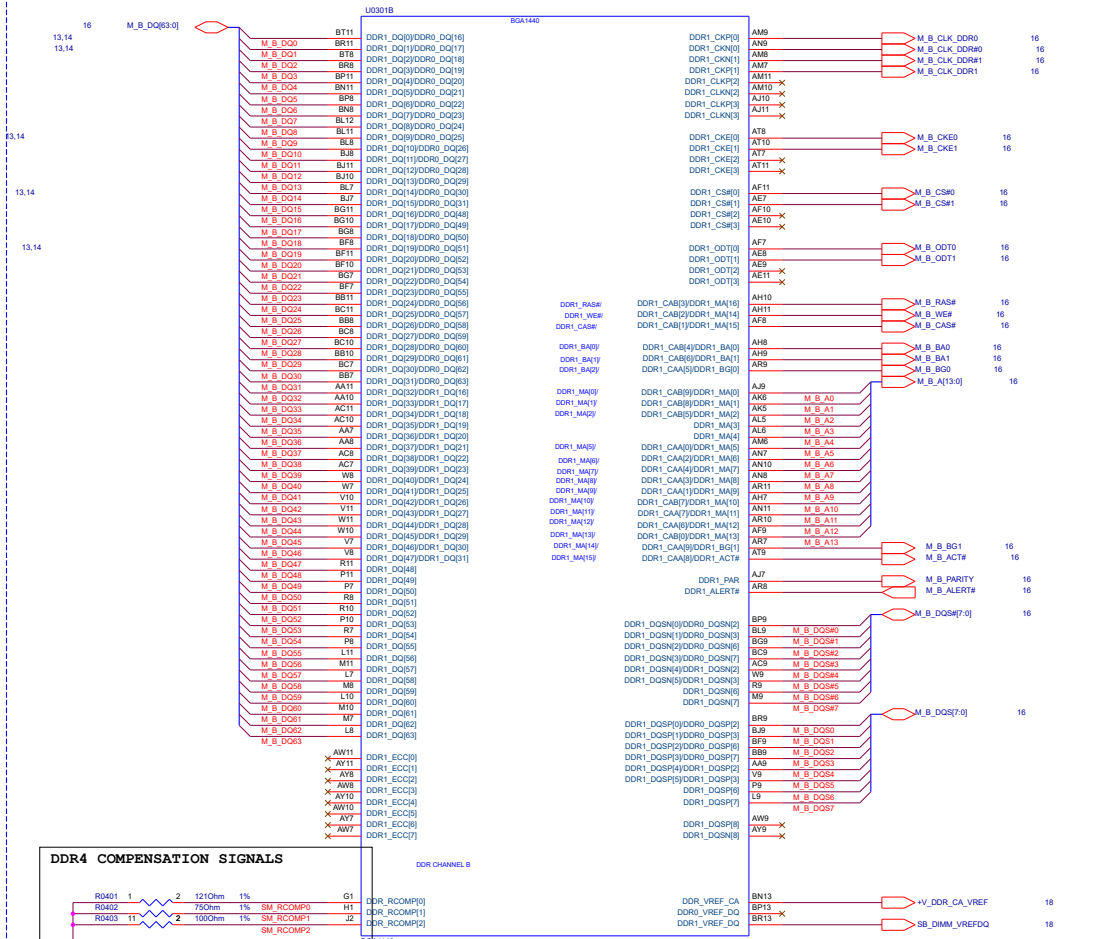


Project Name: GL502			Rev: 1.0
Title : CPU_DMI,PEG,FDI,eDP,DDI			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 3 of 102		

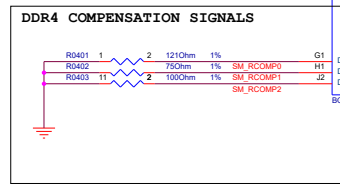
Memory Channel A



Memory Channel B



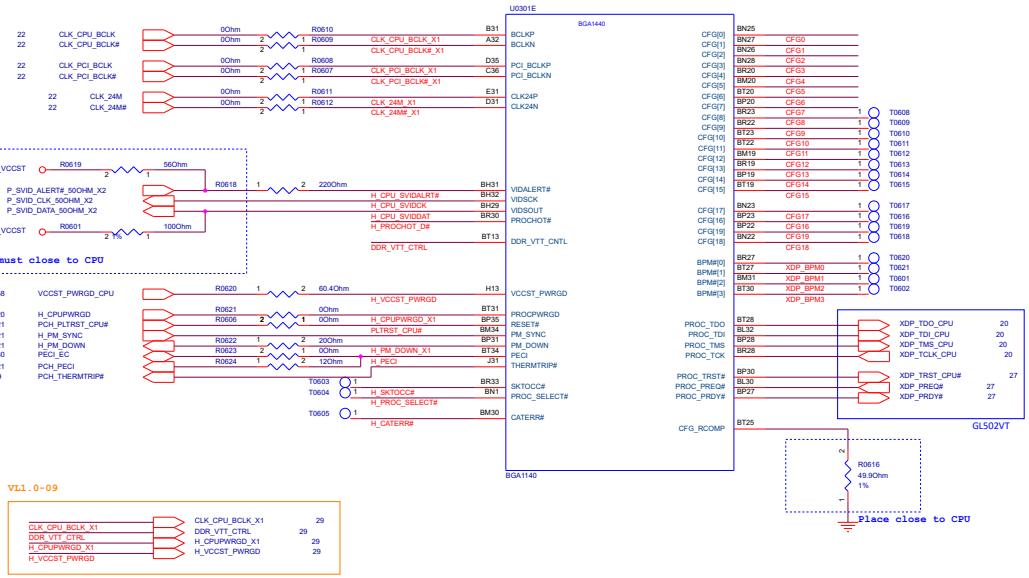
DDR4 COMPENSATION SIGNALS



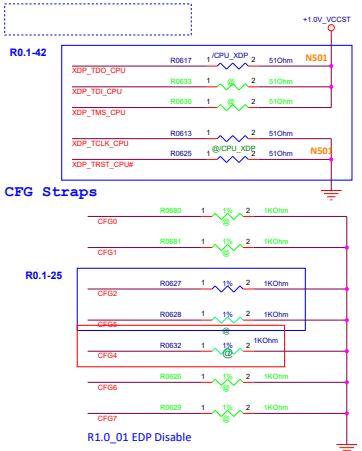
DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ
BN13
BP13
BR13
+V_DDR_CA_VREF 18
SB_DIMM_VREFDQ 18

ASUS	Project Name: N501VW	Rev: 1.0
Title : CPU_DDR4		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Monday, July 25, 2016	Sheet 4 of 102	

CFG



CFG Straps



CFG Straps for Processor

ref : Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

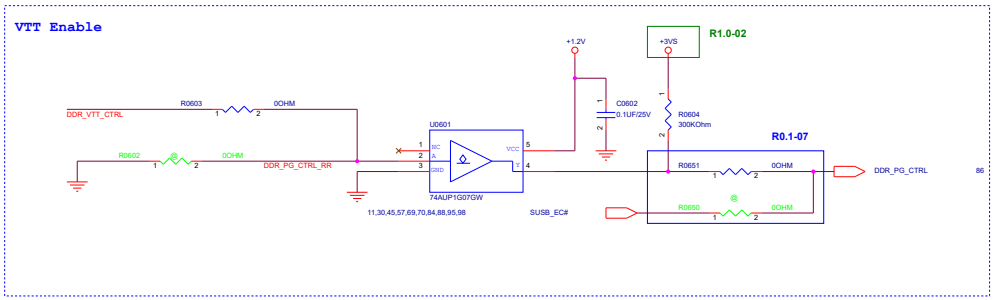
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

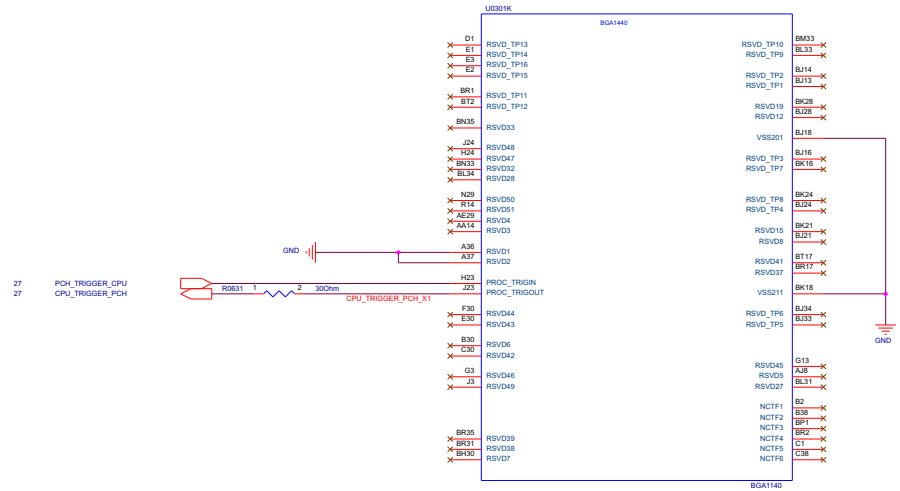
CFG[19:8] : Reserved Configuration Lanes

Reserved Configuration Lanes

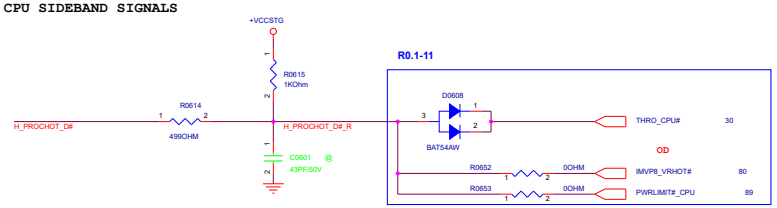
Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121
Richard 2014I209

DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120





CPU SIDEBAND SIGNALS

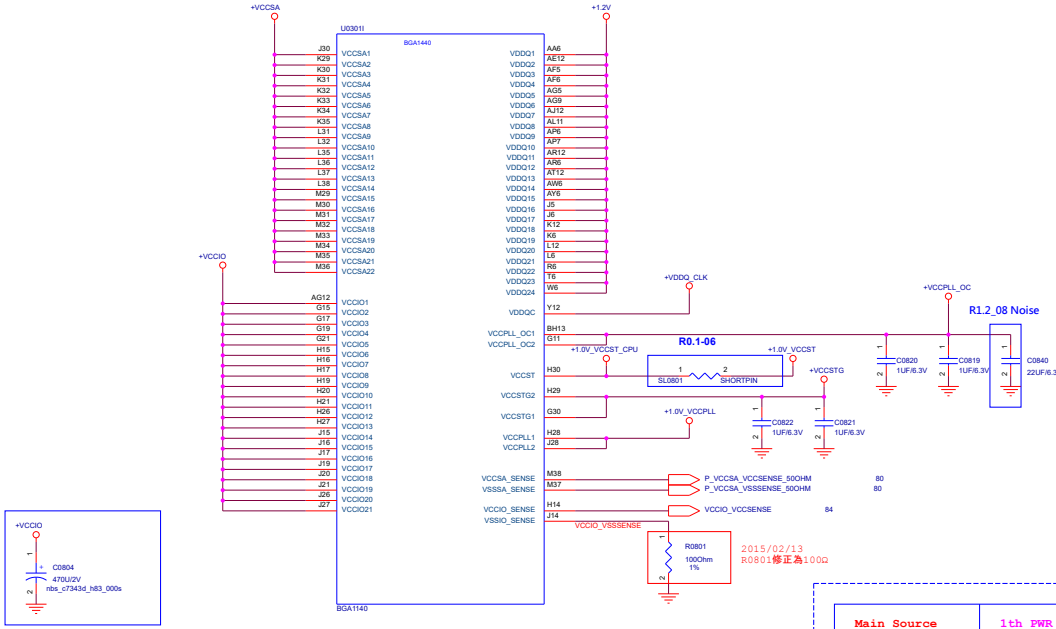


ASUS	Project Name: GL502		Rev: 1.0
Title : NB_****			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 6 of 102		

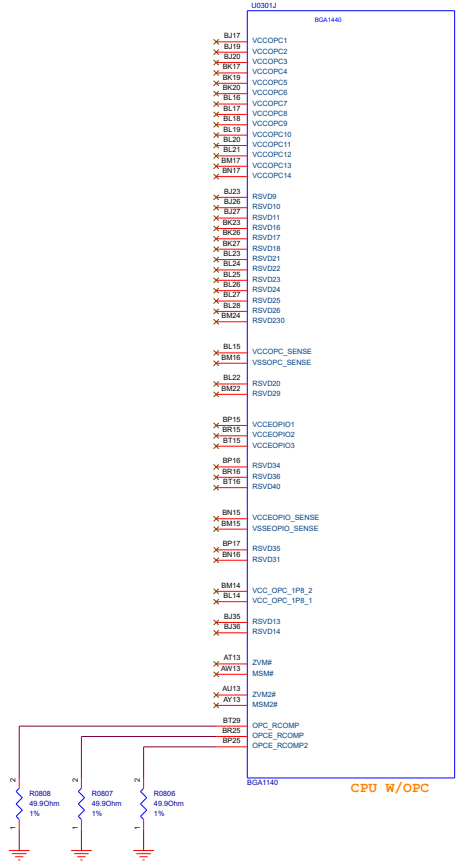
ASUS	Project Name: GL502	Rev: 1.0
Title : CPU XDP		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1
Date: Monday, July 25, 2016	Sheet 7 of 102	

Main Board

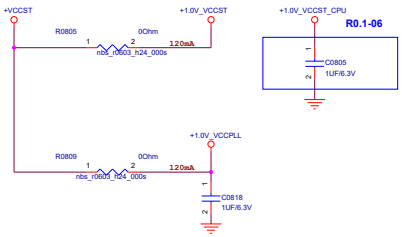
OPC Power Rails



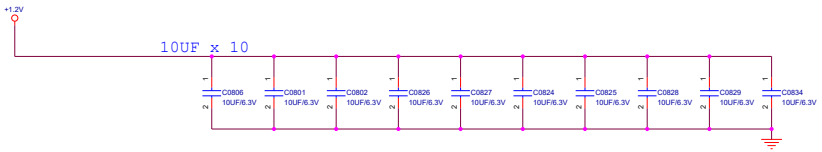
Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.0VSUS	+VCCST	+1.0V_VCCST
			+1.0V_VCCPLL
	+1.2V	+VDDQ_CPU	+VDDQ_CLK
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO	+VCCSTG	



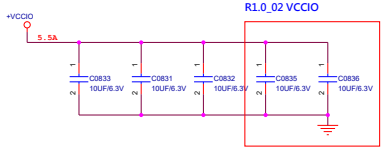
+1.0V_VCCST/+1.0V_VCCPLL DECAPS Place Back Side (TOP)



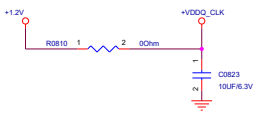
+VDDQ DECAPS Place Back Side (TOP)



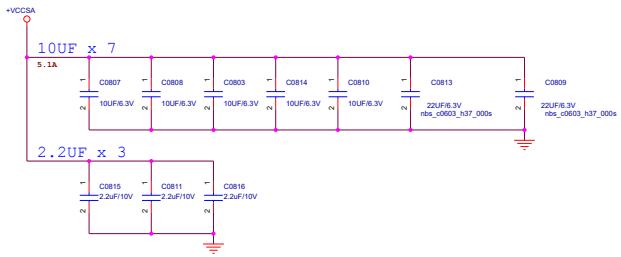
+VCCIO DECAPS Place Back Side (TOP)

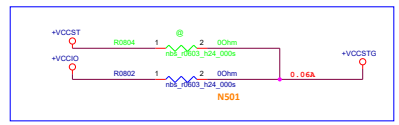


+VDDQ_CLK DECAPS Place Back Side (TOP)



+VCCSA DECAPS Place Back Side (TOP)





Volume Segment
+VCCIO is supplied +1.0VS (shared with +VCCSTG)

ASUS	Project Name: GL502		Rev: 1.0
Title : CPU_PWR			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 8 of 102		

For W/GT3/GT4 CPU

U0301N

BGA1440

AJ29	VCCGT1	VCCGTX1	AF29
AJ30	VCCGT2	VCCGTX2	AF30
AJ31	VCCGT3	VCCGTX3	AF31
AJ32	VCCGT4	VCCGTX4	AF32
AJ33	VCCGT5	VCCGTX5	AF33
AJ34	VCCGT6	VCCGTX6	AF34
AJ35	VCCGT7	VCCGTX7	AG13
AJ36	VCCGT8	VCCGTX8	AG14
AK31	VCCGT9	VCCGTX9	AG31
AK32	VCCGT10	VCCGTX10	AG32
AK33	VCCGT11	VCCGTX11	AG33
AK34	VCCGT12	VCCGTX12	AG34
AK35	VCCGT13	VCCGTX13	AG35
AK36	VCCGT14	VCCGTX14	AG36
AK37	VCCGT15	VCCGTX15	AH13
AK38	VCCGT16	VCCGTX16	AH14
AL13	VCCGT17	VCCGTX17	AH29
AL29	VCCGT18	VCCGTX18	AH30
AL30	VCCGT19	VCCGTX19	AH31
AL31	VCCGT20	VCCGTX20	AH32
AL32	VCCGT21	VCCGTX21	AJ13
AL35	VCCGT22	VCCGTX22	AJ14
AL36	VCCGT23		
AL37	VCCGT24		
AL38	VCCGT25		
AM13	VCCGT26		
AM14	VCCGT27		
AM29	VCCGT28		
AM30	VCCGT29		
AM31	VCCGT30		
AM32	VCCGT31		
AM33	VCCGT32		
AM34	VCCGT33		
AM35	VCCGT34		
AM36	VCCGT35		
AN13	VCCGT36		
AN14	VCCGT37		
AN31	VCCGT38		
AN32	VCCGT39		
AN33	VCCGT40		
AN34	VCCGT41		
AN35	VCCGT42		
AN36	VCCGT43		
AN37	VCCGT44		
AN38	VCCGT45		
AP13	VCCGT46		
AP14	VCCGT47		
AP29	VCCGT48		
AP30	VCCGT49		
AP31	VCCGT50		
AP32	VCCGT51		
AP35	VCCGT52		
AP36	VCCGT53		
AP37	VCCGT54		
AP38	VCCGT55		
AR29	VCCGT56		
AR30	VCCGT57		
AR31	VCCGT58		
AR32	VCCGT59		
AR33	VCCGT60	VCCGT_SENSE	AH38
AR34	VCCGT61	VSSGTX_SENSE	AH35
AR35	VCCGT62	VSSGT_SENSE	AH37
AR36	VCCGT63	VCCGTX_SENSE	AH36
AT14	VCCGT64		
AT31	VCCGT65		
AT32	VCCGT66		
AT33	VCCGT67		
AT34	VCCGT68		
AT35	VCCGT69		
AT36	VCCGT70		
AT37	VCCGT71		
AT38	VCCGT72		
AU14	VCCGT73		
AU29	VCCGT74		
AU30	VCCGT75		
AU31	VCCGT76		
AU32	VCCGT77		
AU35	VCCGT78		
AU36	VCCGT79		
AU37	VCCGT80		
AU38	VCCGT81		

BGA1140

U0301H

BGA1440

BG34	VCCGT168	VCCGT82	AV29
BG35	VCCGT169	VCCGT83	AV30
BG36	VCCGT170	VCCGT84	AV31
BH33	VCCGT171	VCCGT85	AV32
BH34	VCCGT172	VCCGT86	AV33
BH35	VCCGT173	VCCGT87	AV34
BH36	VCCGT174	VCCGT88	AV35
BH37	VCCGT175	VCCGT89	AV36
BH38	VCCGT176	VCCGT90	AW14
BJ37	VCCGT177	VCCGT91	AW31
BJ38	VCCGT178	VCCGT92	AW32
BL36	VCCGT179	VCCGT93	AW33
BL37	VCCGT180	VCCGT94	AW34
BM36	VCCGT181	VCCGT95	AW35
BM37	VCCGT182	VCCGT96	AW36
BN36	VCCGT183	VCCGT97	AW37
BN37	VCCGT184	VCCGT98	AW38
BN38	VCCGT185	VCCGT99	AY29
BP37	VCCGT186	VCCGT100	AY30
BP38	VCCGT187	VCCGT101	AY31
BR37	VCCGT188	VCCGT102	AY32
BT37	VCCGT189	VCCGT103	AY35
BE38	VCCGT152	VCCGT104	AY36
BF13	VCCGT153	VCCGT105	AY37
BF14	VCCGT154	VCCGT106	AY38
BF29	VCCGT155	VCCGT107	BA13
BF30	VCCGT156	VCCGT108	BA14
BF31	VCCGT157	VCCGT109	BA29
BF32	VCCGT158	VCCGT110	BA30
BF35	VCCGT159	VCCGT111	BA31
BF36	VCCGT160	VCCGT112	BA32
BF37	VCCGT161	VCCGT113	BA33
BF38	VCCGT162	VCCGT114	BA34
BG29	VCCGT163	VCCGT115	BA35
BG30	VCCGT164	VCCGT116	BA36
BG31	VCCGT165	VCCGT117	BB13
BG32	VCCGT166	VCCGT118	BB14
BG33	VCCGT167	VCCGT119	BB31
BC36	VCCGT132	VCCGT120	BB32
BC37	VCCGT133	VCCGT121	BB33
BC38	VCCGT134	VCCGT122	BB34
BD13	VCCGT135	VCCGT123	BB35
BD14	VCCGT136	VCCGT124	BB36
BD29	VCCGT137	VCCGT125	BB37
BD30	VCCGT138	VCCGT126	BB38
BD31	VCCGT139	VCCGT127	BC29
BD32	VCCGT140	VCCGT128	BC30
BD33	VCCGT141	VCCGT129	BC31
BD34	VCCGT142	VCCGT130	BC32
BD35	VCCGT143	VCCGT131	BC35
BD36	VCCGT144	VCCGT147	BE33
BE31	VCCGT145	VCCGT148	BE34
BE32	VCCGT146	VCCGT149	BE35
BE37	VCCGT151	VCCGT150	BE36

BGA1140

+VCCCORE

+VCCCORE

U0301G

BGA1440

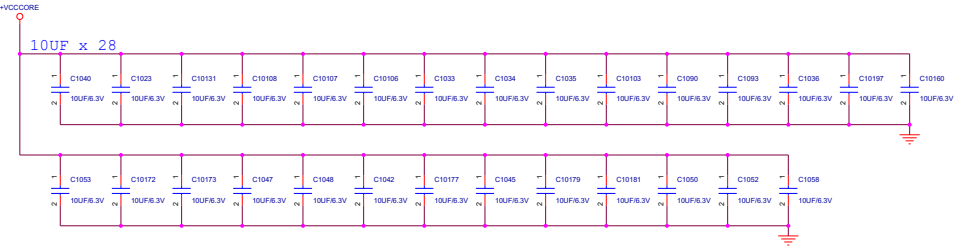
AA13	VCC1	VCC102	V32
AA31	VCC2	VCC103	V33
AA32	VCC3	VCC104	V34
AA33	VCC4	VCC105	V35
AA34	VCC5	VCC106	V36
AA35	VCC6	VCC107	V37
AA36	VCC7	VCC108	V38
AA37	VCC8	VCC109	W13
AA38	VCC9	VCC110	W14
AB29	VCC10	VCC111	W29
AB30	VCC11	VCC112	W30
AB31	VCC12	VCC113	W31
AB32	VCC13	VCC114	W32
AB35	VCC14	VCC115	W35
AB36	VCC15	VCC116	W36
AB37	VCC16	VCC117	W37
AB38	VCC17	VCC118	W38
AC13	VCC18	VCC119	Y29
AC14	VCC19	VCC120	Y30
AC29	VCC20	VCC121	Y31
AC30	VCC21	VCC122	Y32
AC31	VCC22	VCC123	Y33
AC32	VCC23	VCC124	Y34
AC33	VCC24	VCC125	Y35
AC34	VCC25	VCC126	Y36
AC35	VCC26	VCC54	L14
AC36	VCC27	VCC66	P29
AD13	VCC28	VCC67	P30
AD14	VCC29	VCC68	P31
AD31	VCC30	VCC69	P32
AD32	VCC31	VCC70	P33
AD33	VCC32	VCC71	P34
AD34	VCC33	VCC72	P35
AD35	VCC34	VCC73	P36
AD36	VCC35	VCC74	R13
AD37	VCC36	VCC75	R31
AD38	VCC37	VCC76	R32
AE13	VCC38	VCC77	R33
AE14	VCC39	VCC78	R34
AE30	VCC40	VCC79	R35
AE31	VCC41	VCC80	R36
AE32	VCC42	VCC81	R37
AE35	VCC43	VCC82	R38
AE36	VCC44	VCC83	T29
AE37	VCC45	VCC84	T30
AE38	VCC46	VCC85	T31
AF35	VCC47	VCC86	T32
AF36	VCC48	VCC87	T35
AF37	VCC49	VCC88	T36
AF38	VCC50	VCC89	T37
K13	VCC51	VCC90	T38
K14	VCC52	VCC91	U29
L13	VCC53	VCC92	U30
N13	VCC55	VCC93	U31
N14	VCC56	VCC94	U32
N30	VCC57	VCC95	U33
N31	VCC58	VCC96	U34
N32	VCC59	VCC97	U35
N35	VCC60	VCC98	U36
N36	VCC61	VCC99	V13
N37	VCC62	VCC100	V14
N38	VCC63	VCC101	V31
P13	VCC64	VCC65	P14

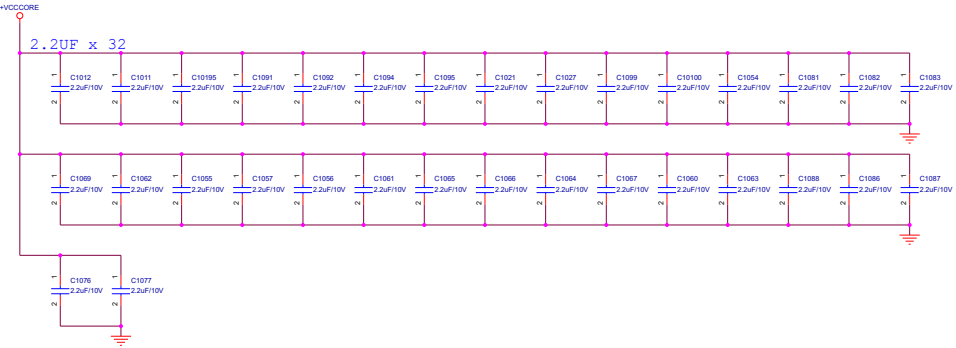
VCC_SENSE	AG37	P_VCCCORE_VCCSENSE_50OHM	80
VSS_SENSE	AG38	P_VCCCORE_VSSSENSE_50OHM	80

BGA1140

ASUS	Project Name: GL502	Rev: 1.0	
Title : NB_****			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 9 of 102		

+VCCORE DECAPS Place Back Side (TOP)





+VCCGT DECAPS Place Back Side (TOP)

ASUS	Project Name: GL502	Rev: 1.0
Title : 010_CPU_POWER_CAP		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1
Date: Monday, July 25, 2016	Sheet 10 of 102	

Main Board

NOTE:
For JTAG Debug

IF SOME OF GPIOs ARE NOT IN USE, FOLLOW TABLE BELOW :

GPIO	Termination	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PD	
GPIO_3	100K PD	
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	
GPIO_7	100K PD	
GPIO_8	100K PD	
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PD	
POC_GPIO_3	100K PD	
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	10K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PD	

NOTE:
ASSEMBLE R1115, R1104 if DPSRC IS NOT IN USE

Alpine-Ridge Flash Memory

PCH_R2506 10Kohm Pull High +3Vs

To PCH GPIO that supports SCI

Low pulse

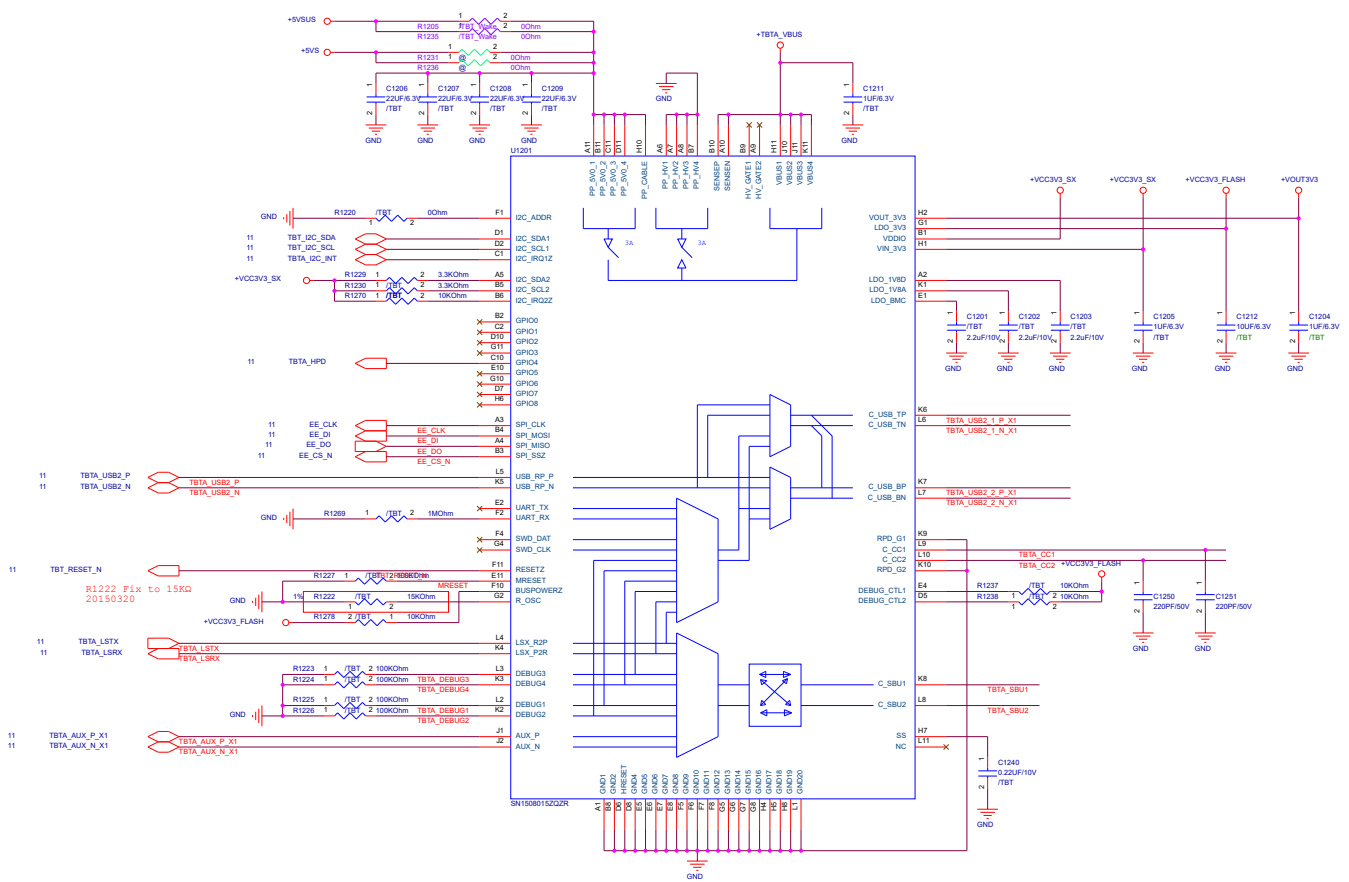
TBT SLP_S3#

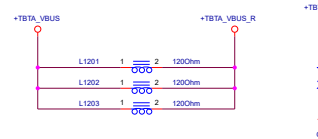
TBT Force PWR

Debug Pin Not Use Setting:

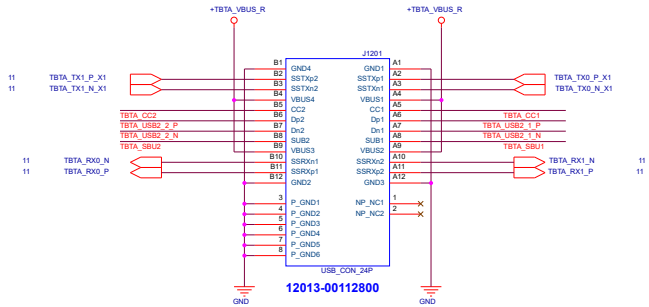
PIN	Termination
MONDC_SVR	GND
MONDC_DPSNK_0	GND
MONDC_DPSNK_1	GND
MONDC_DPSRC	GND
MONDC_CIO_0	GND
MONDC_CIO_1	GND
TEST_EDM	GND
FUSE_VQPS_64	GND
FUSE_VQPS_128	GND
ATEST_P/N	FLOATING
USB2_ATEST	FLOATING
PCIE_ATEST	FLOATING

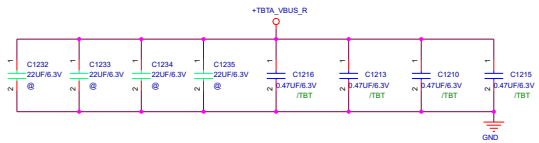
Project Name	GL702VT
Rev	1.0
Title :	Intel Alpine-Ridge
Size	
Dept.:	ASUSTeK COMPUTER INC
Engineer:	Eric Chuang
Date: Monday, July 25, 2016	Sheet 11 of 102

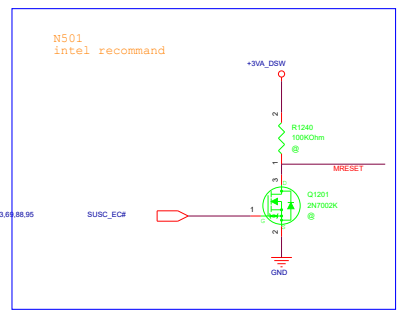




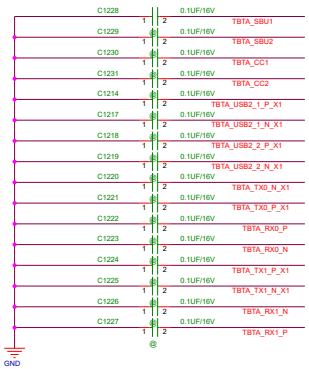
USB type C

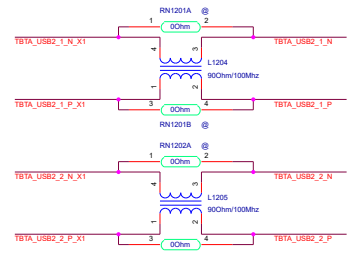




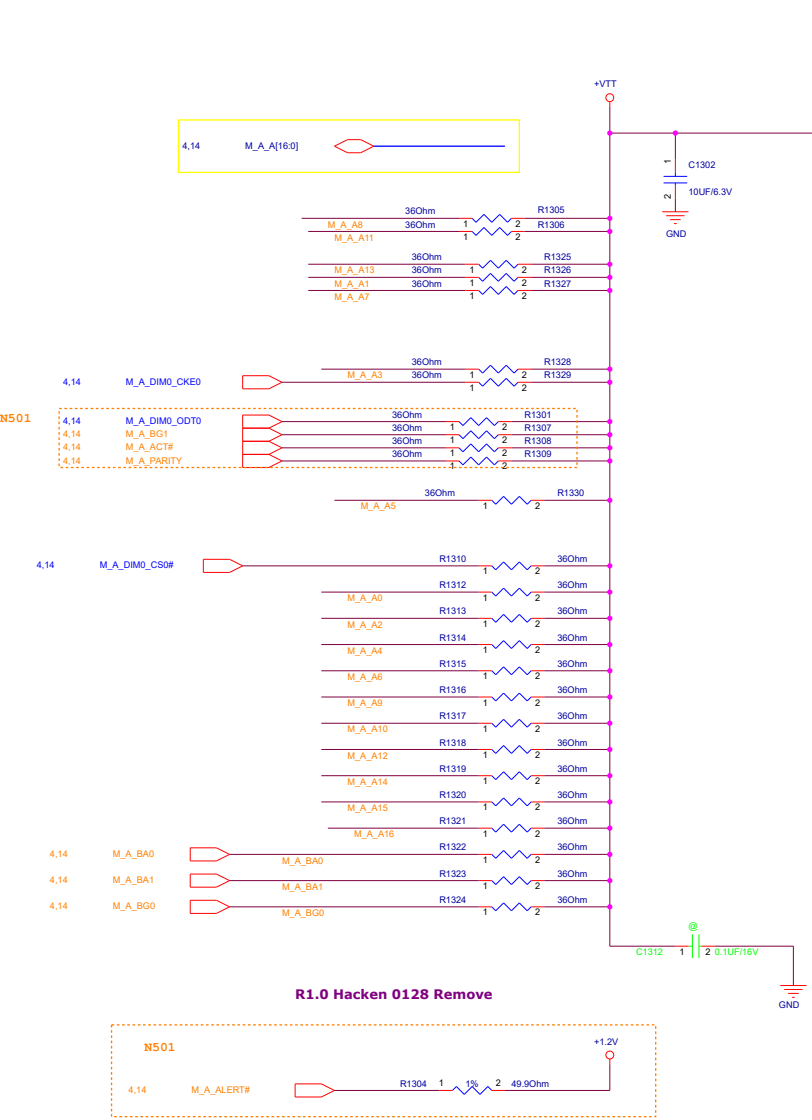


ESD-Protection

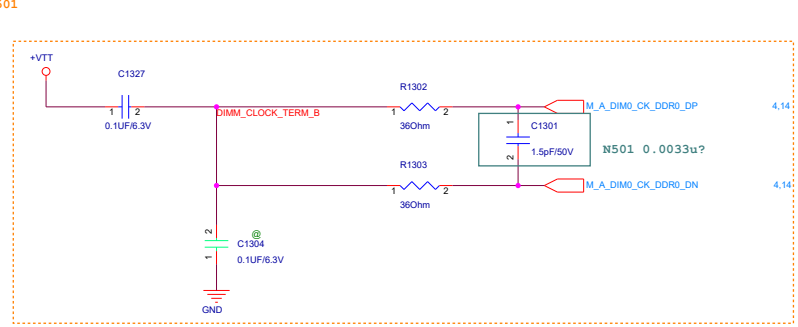




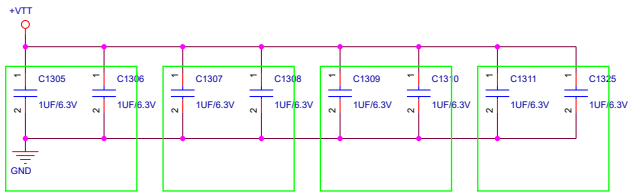
ASUS	Project Name: GL702VT		Rev: 1.0
Title :	TPS65982 & USB 3.1 Type-C		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Eric Chuang	
Date: Monday, July 25, 2016	Sheet 12 of 102		

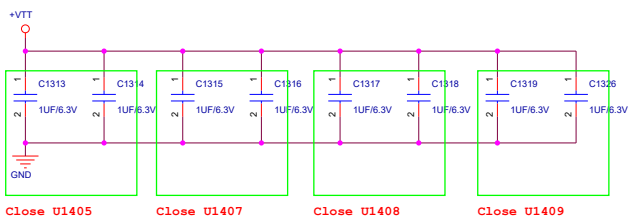


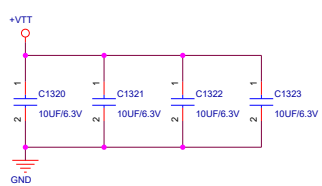
R1.0 Hacken 0128 Remove



3.Page13.Delete C1309 and Clock Pull up power change from +1.2V to +0.6V -20121212







DDR4_TERMINATION

EE

ASUSTeK COMPUTER INC.

Custom N501VW 1.0

Monday, July 25, 2016 13 102

<Variant Name>

DDR4_ON-BOARD_A2

ASUSTeK COMPUTER INC.

EE

Custom

N501VW

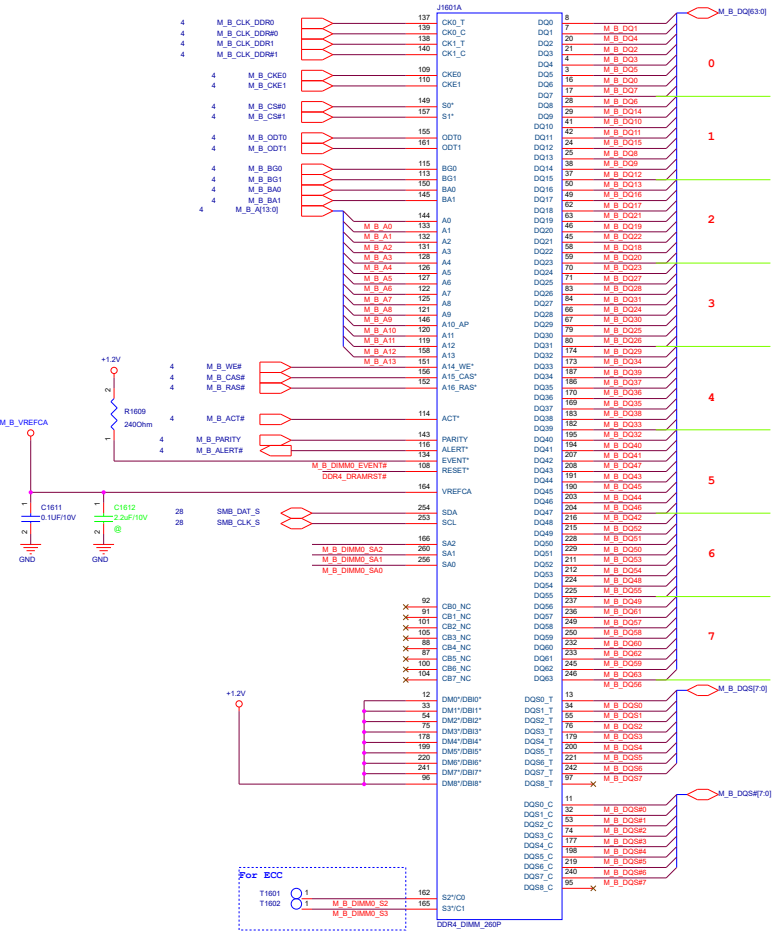
1.0

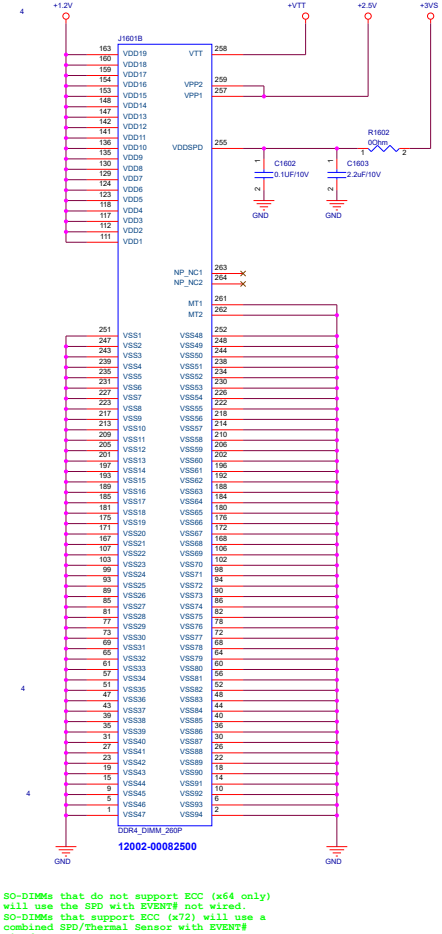
Monday, July 25, 2016

15

102

SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)

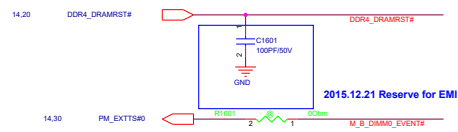


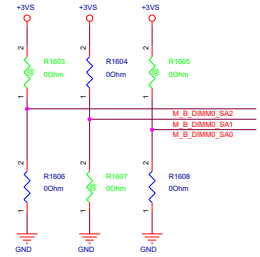


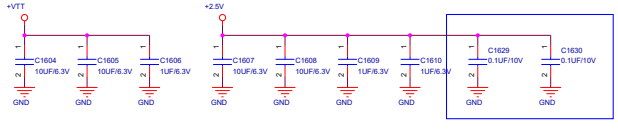
SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

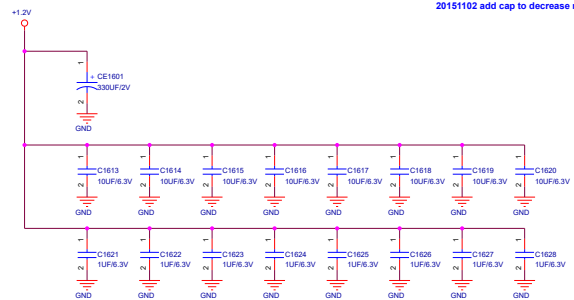
EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

Main Board









ASUS	Project Name: N501VW		Rev: 1.0
Title :	DIM_DDR4 SO-DIMM B1		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Monday, July 25, 2016	Sheet 16 of 102		

<Variant Name>

NB_****

EE

ASUSTeK COMPUTER INC. NB1

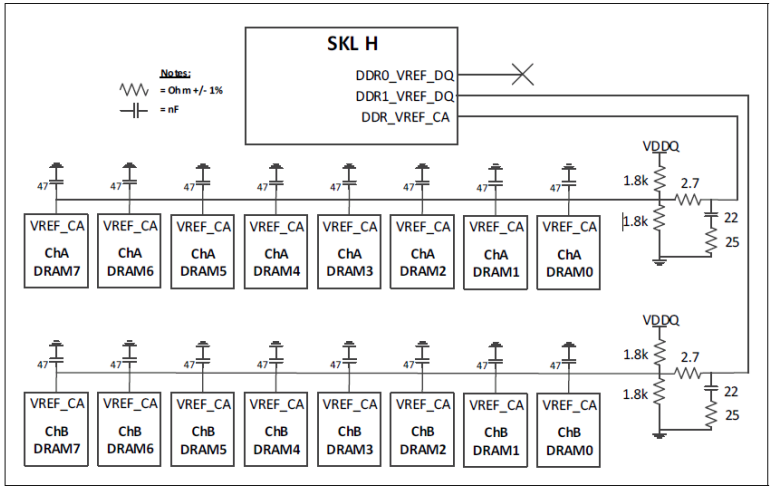
A

N501VW

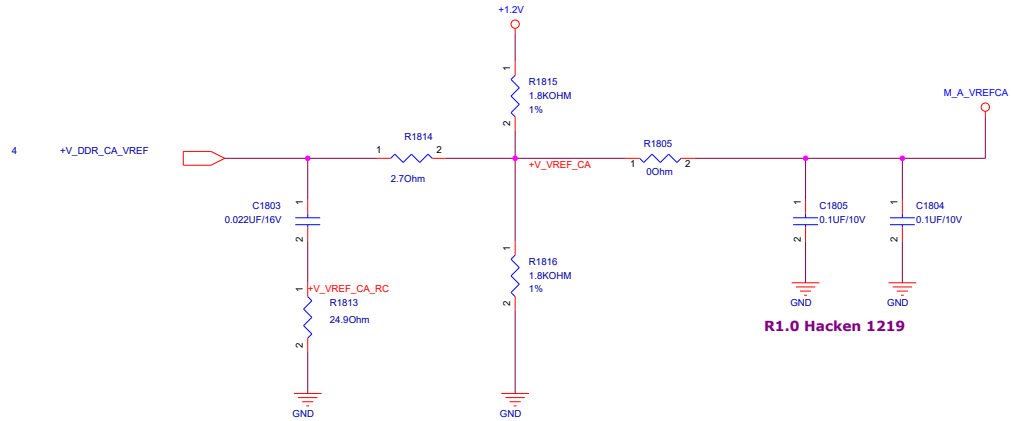
1.0

Monday, July 25, 2016

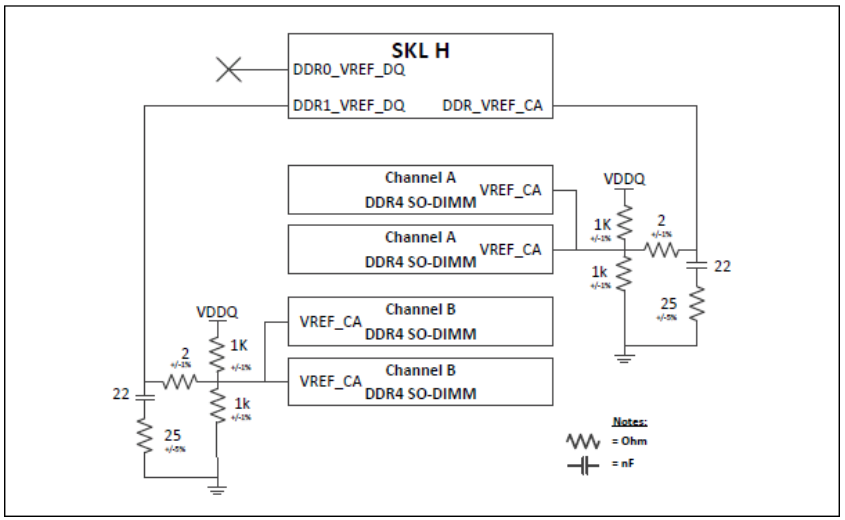
Figure 4-27. SKL H DDR4/DDR4-RS x8 Memory Down V_{REF-CA} Overview



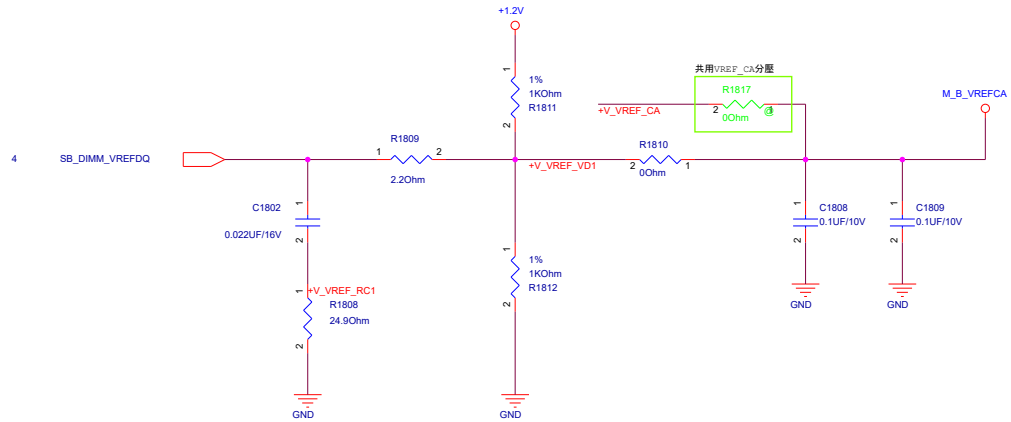
SO-DIMM0 Vref



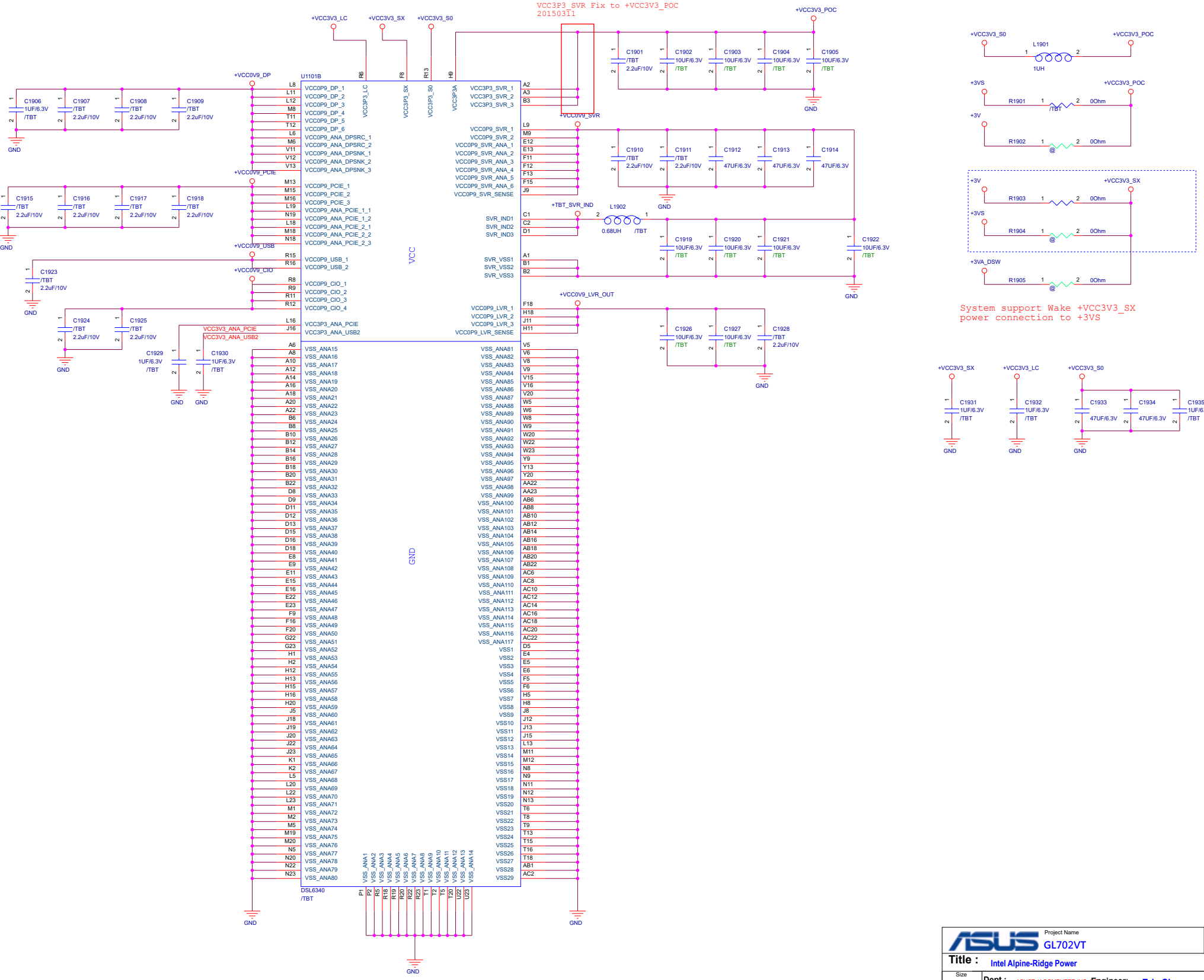
SKL H DDR4/DDR4-RS SO-DIMM V_{REF-CA} Overview



SO-DIMM1 Vref



Project Name: N501VW		Rev: 1.0
Title: DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Monday, July 25, 2016	Sheet 18 of 102	

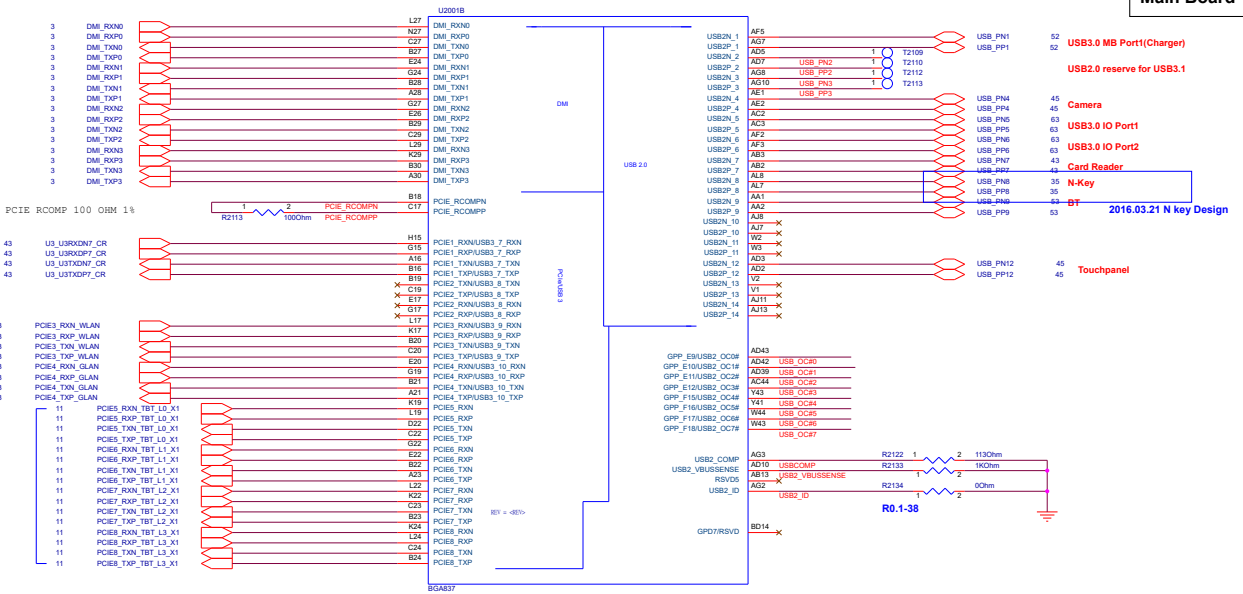


Project Name: GL702VT			Rev: 1.0
Title: Intel Alpine-Ridge Power			
Size: Custom	Dept.: ASUSTeK COMPUTER INC. (BU	Engineer: Eric Chuang	
Date: Monday, July 25, 2016	Sheet 19 of 102		

PCIE Setting

GL502VM PCIE/SATA Function define
Skylake HM170

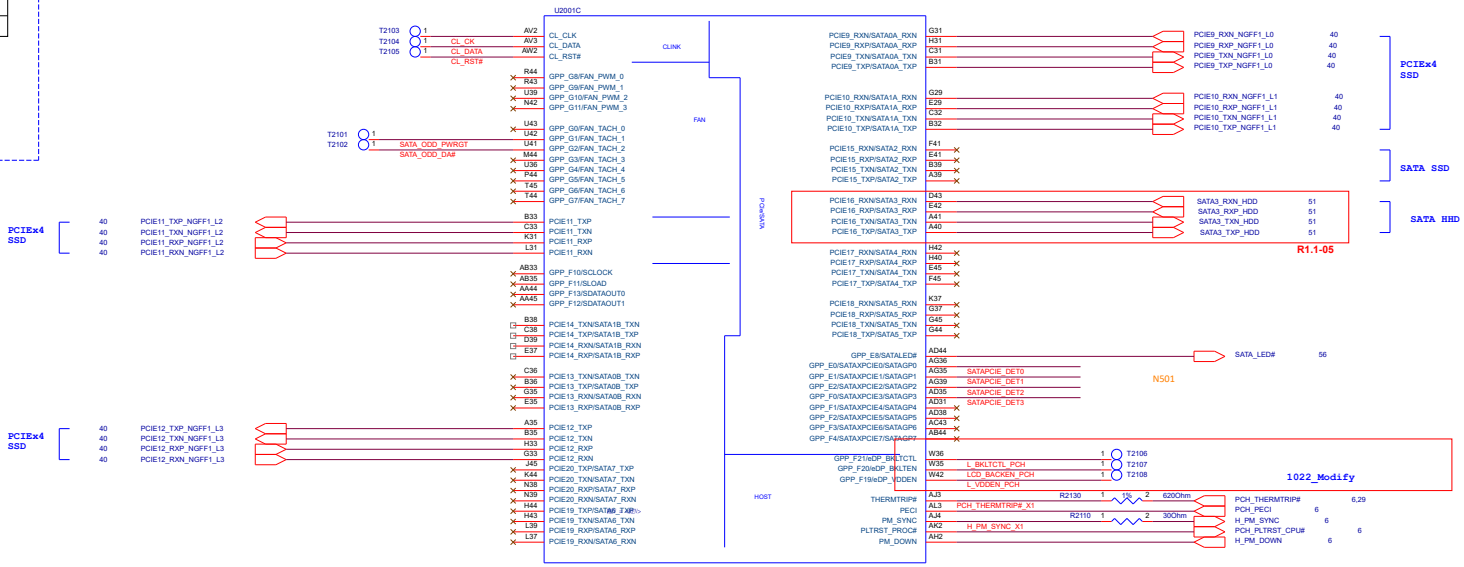
HSIO	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3_IO	
02	USB3#02 / SSIC#01		
03	USB3#03 / SSIC#02		
04	USB3#04		
05	USB3#05	USB3_IO	
06	USB3#06	USB3_IO	
07	USB3#07 / PCIE#01	CardReader_USB3	SRC1
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	GLAN	SRC4
11	PCIE#05 / GBE	TBT	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	PCIE*4 SSD SATA SSD	SRC6
16	PCIE#10 / SATA#1		
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3	1st HDD	
23			
24			
25			
26			



USB Setting

GL502VM USB Function define
Skylake HM170

USB 2.0	Function	USB 3.0	Function
USB2_01	USB3.0 MB Port1	USB3_01	MB USB3.0
USB2_02		USB3_02	
USB2_03		USB3_03	
USB2_04	Camera	USB3_04	
USB2_05	USB3.0 IO Port1	USB3_05	USB3.0 IO Port1
USB2_06	USB3.0 IO Port2	USB3_06	USB3.0 IO Port2
USB2_07	CardReader	USB3_07	Card reader
USB2_08	N-Key	USB3_08	
USB2_09	BT		
USB2_10			
USB2_11			
USB2_12			

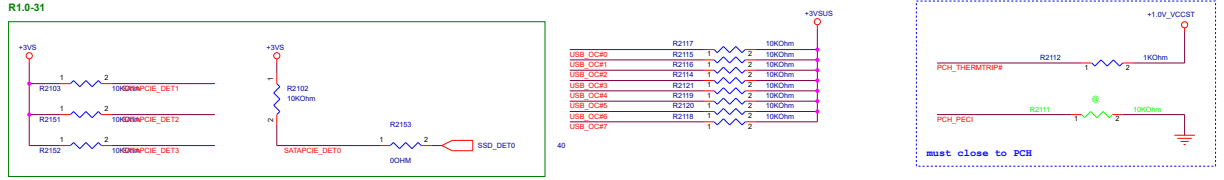


N501VW PCIE/SATA Function define

	Function
PCIE-01	
PCIE-02	
PCIE-03	WLAN
PCIE-04	GLAN
PCIE-05	TBT AR
PCIE-06	TBT AR
PCIE-07	TBT AR
PCIE-08	TBT AR
PCIE-09 (SATA-0A)	PCIE SSD
PCIE-10 (SATA-1A)	PCIE SSD
PCIE-11	PCIE SSD
PCIE-12	PCIE SSD

	Function
PCIE-13 (SATA-0B)	
PCIE-14 (SATA-1B)	
PCIE-15 (SATA-2)	
PCIE-16 (SATA-3)	HDD
PCIE-17 (SATA-4)	
PCIE-18 (SATA-5)	
PCIE-19 (SATA-6)	
PCIE-20 (SATA-7)	

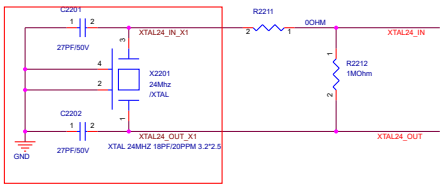
	Function
CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	
CLKREQ-3	WLAN
CLKREQ-4	GLAN
CLKREQ-5	TBT AR
CLKREQ-6	PCIE SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	



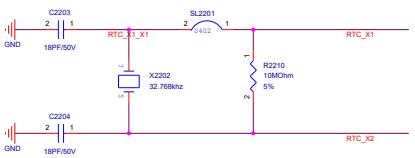
ASUS	Project Name: GL502		Rev: 1.0
Title :	PCH-CPT(2)_PCIE,CLK,USB		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 21 of 102		

XTAL 24MHz

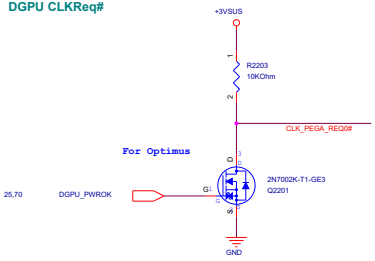
R1.2_15 TXC Suggest



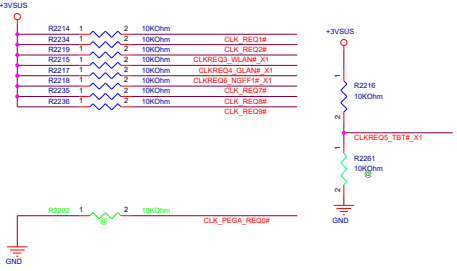
RTC CRYSTAL 32.768KHz

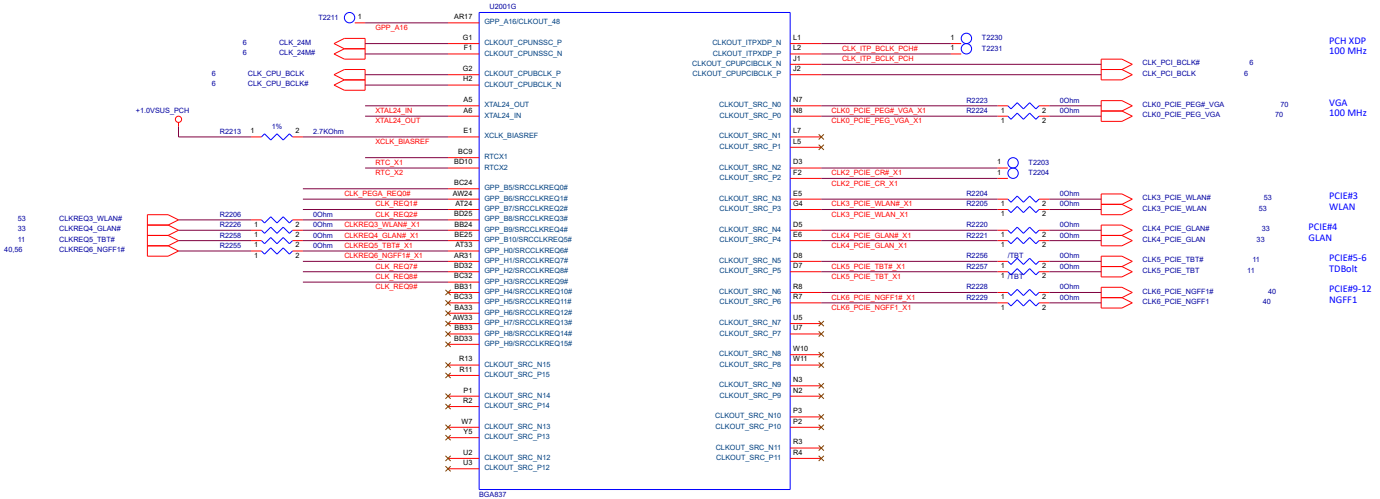


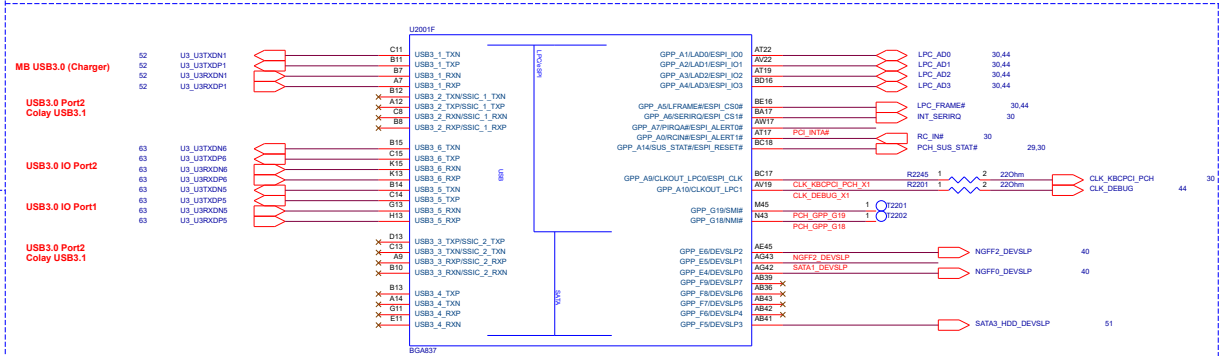
DGPU CLKReq#

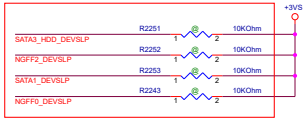


PCH CLKREQ Setting:

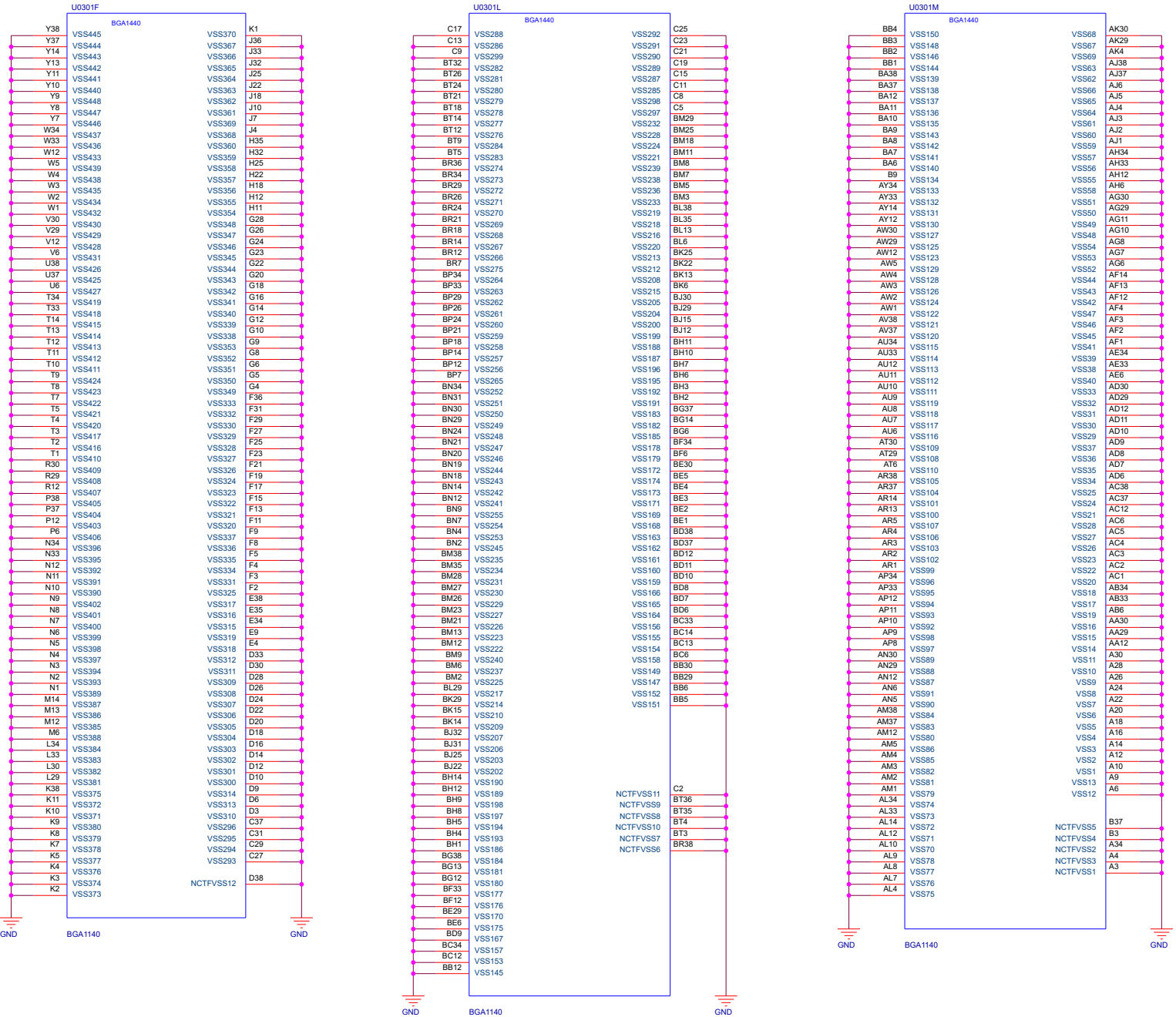








ASUS	Project Name: GL502		Rev: 1.0
Title :	PCH-CPT(3)_FDI,DMI,SYS PWR		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 22 of 102		



Project Name	GL502
Rev	1.0
Title :	CPU_CFG,RSVD,GND
Size	B
Dept.:	ASUSTeK COMPUTER
Engineer:	RD1_EE1
Date:	Monday, July 25, 2016
Sheet	5 of 102

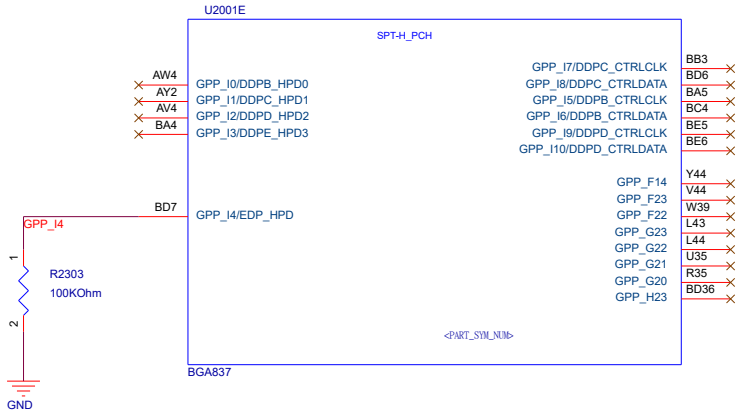
HPD0 to DP

HPD1 to HDMI

HPD2 to TBT

HPD3 to VGA

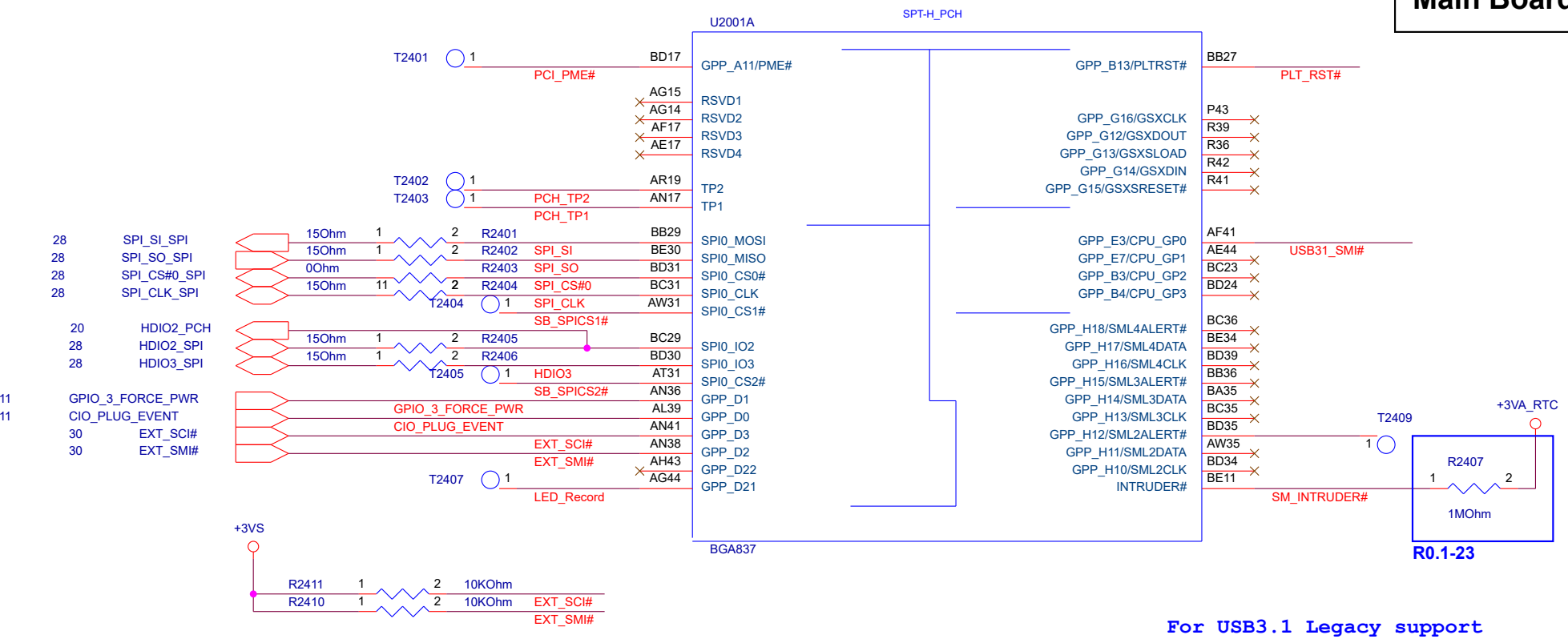
HPD4 to EDP Panel



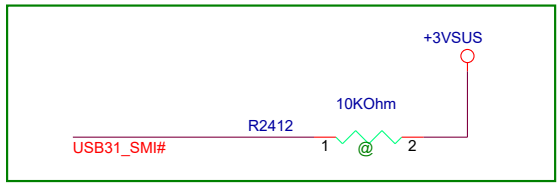
REV = <REV>

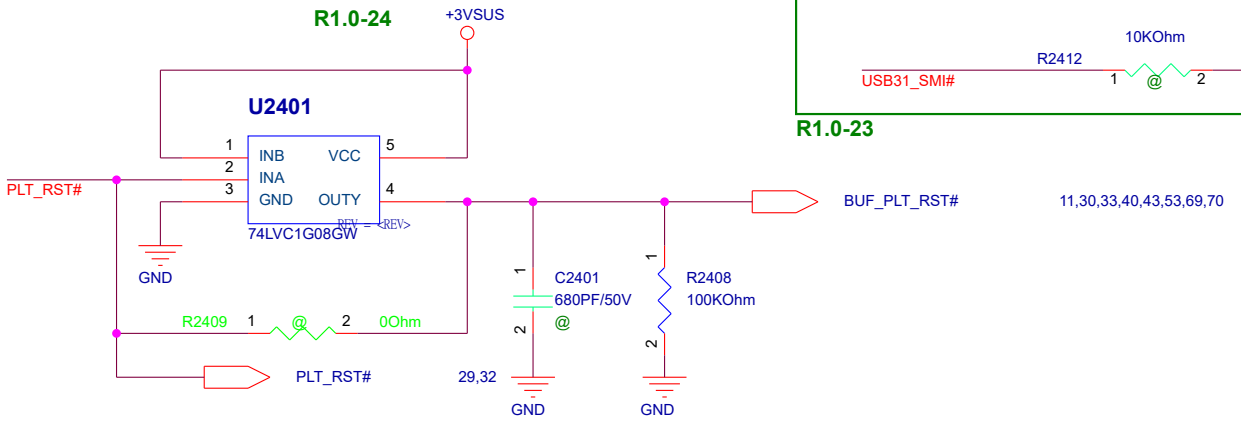
ASUS	Project Name: GL502		Rev: 1.0
Title : PCH-CPT(4)_eDP,PCI,DP			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 23 of 102		

Main Board

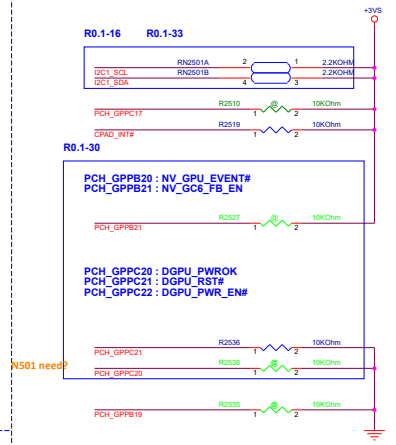


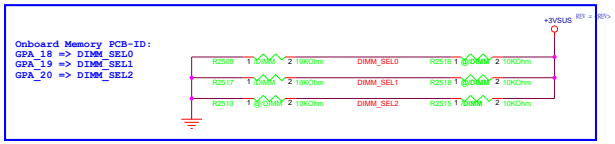
For USB3.1 Legacy support



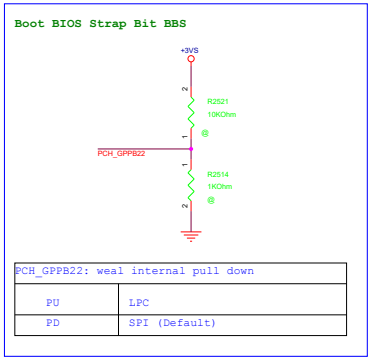


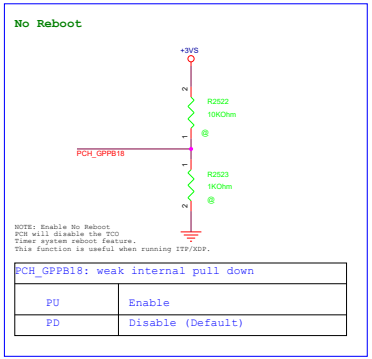
Project Name: GL502		Rev: 1.0
Title : PCH-CPT(5)_LPC,SPI,SMBUS		
Size: A	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1
Date: Monday, July 25, 2016	Sheet 24 of 102	

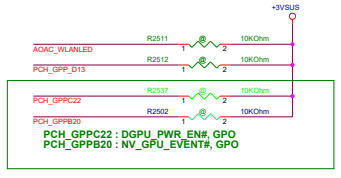


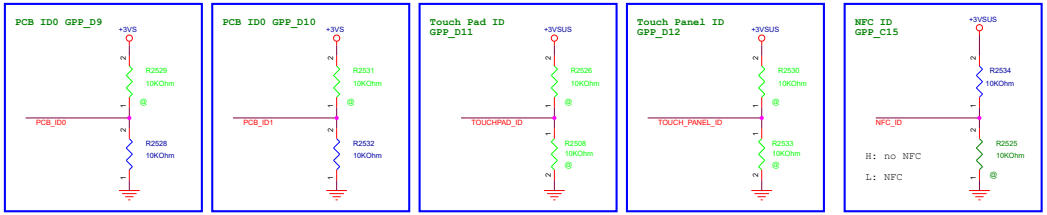


	MIcron (8Gb) 03012-00030100 DDR4 2400 1024M*8 1.2V MT40A1G8SNW-083E:A	Samsung (8Gb) 03012-00030000 DDR4 2133 1024M*8 1.2V FBGA78 K4A8G085WB-BCPB		
DIMM_SEL0	L	L		
DIMM_SEL1	L	L		
DIMM_SEL2	L	H		

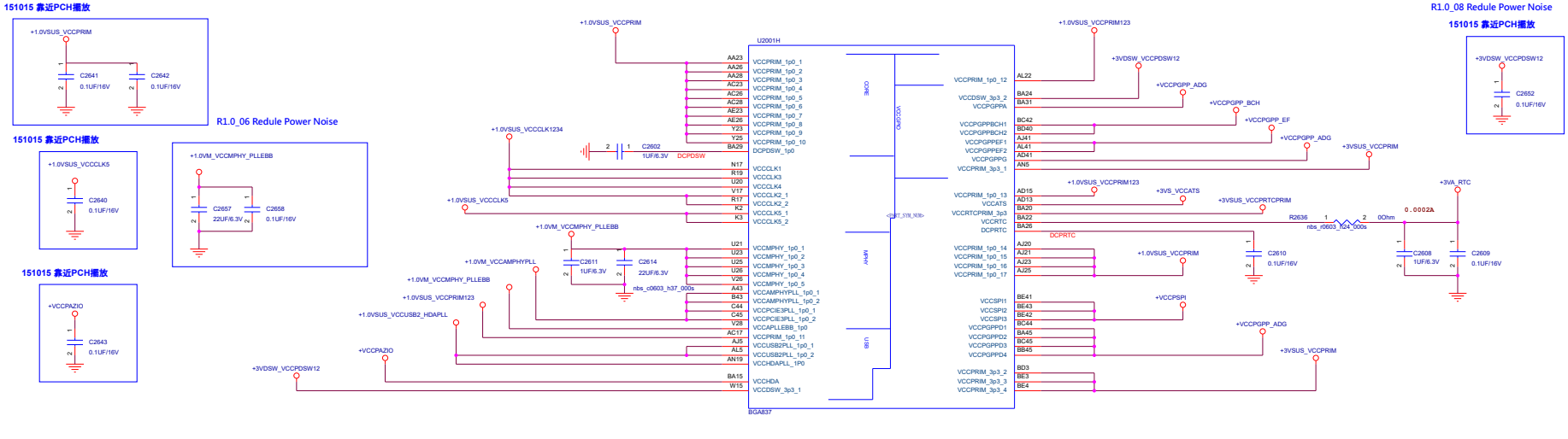


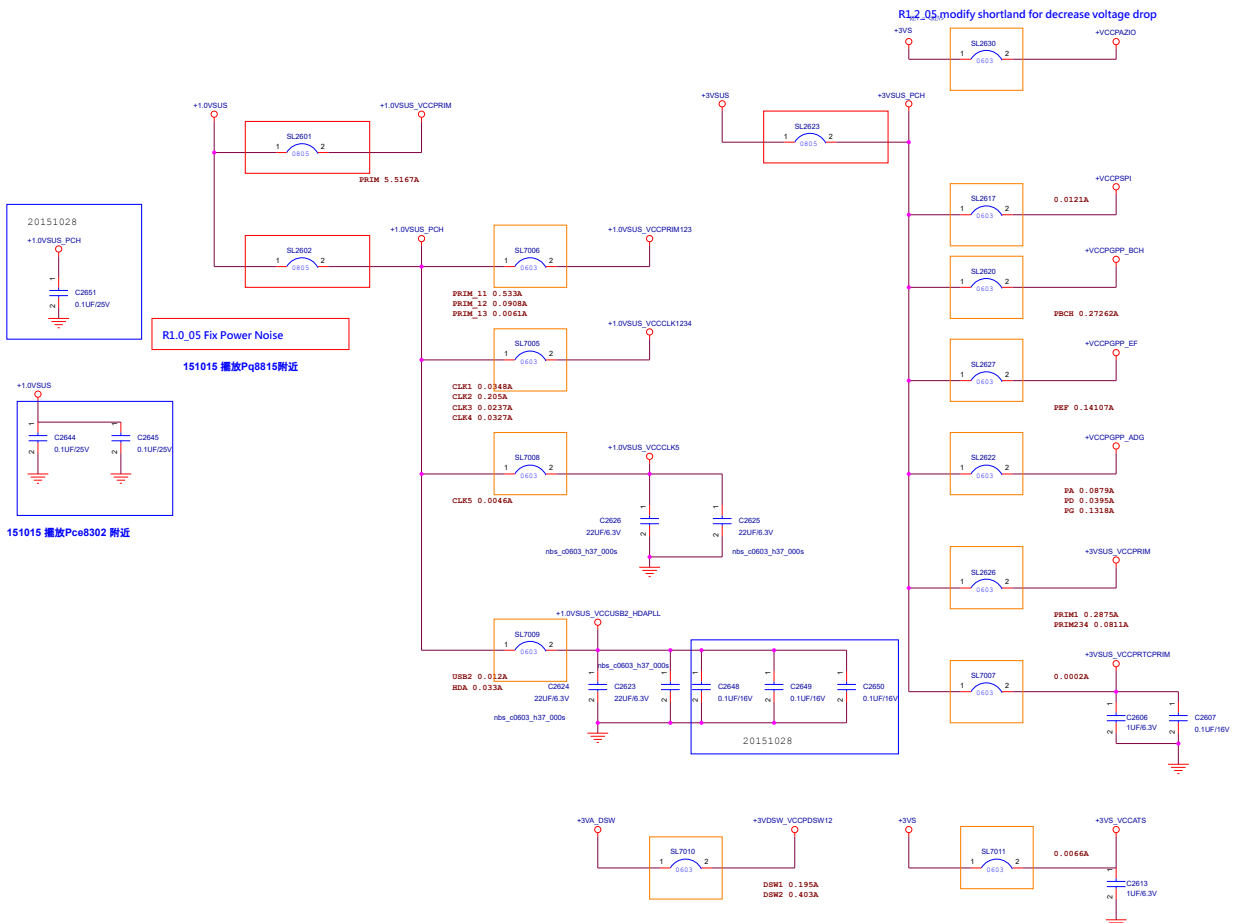


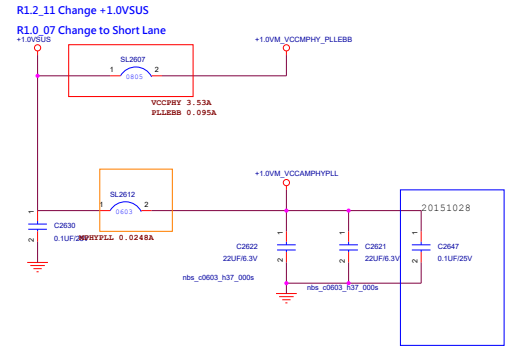




ASUS	Project Name: GL502		Rev: 1.0
Title :	PCH-CPT(6)_GPIO,MISC		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 25 of 102		



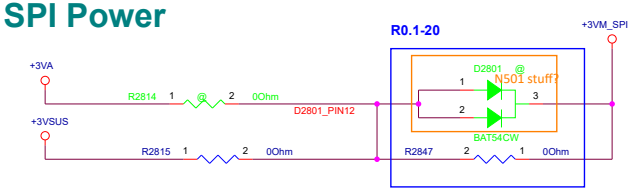


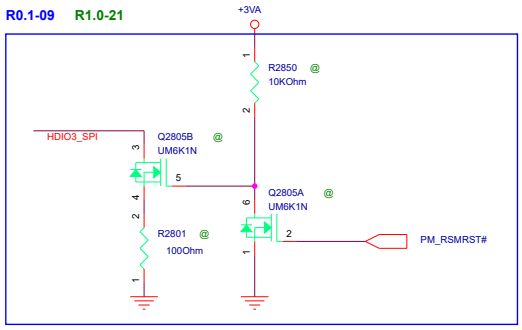


Supply	Value	Quantity	Type	Notes	Placement
VccMPHYPLL & VccPCIE3PLL (Pin A43, B43, C44, C45) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	Recommended to be placed <3 mm from edge of package
	22 uF	2	Filter Capacitor (Vss) 0805	20%	
VccUSB2PLL & VccHDAPLL (Pin AJ5, AL5, AN19) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	
	22 uF	2	Filter Capacitor (Vss) 0805	20%	
VccCLK5 (Pin K2, K3) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	
	22 uF	2	Filter Capacitor (Vss) 0805	20%	

ASUS	Project Name: GL502		Rev: 1.0
Title : PCH-CPT(7)_POWER,GND			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 26 of 102		

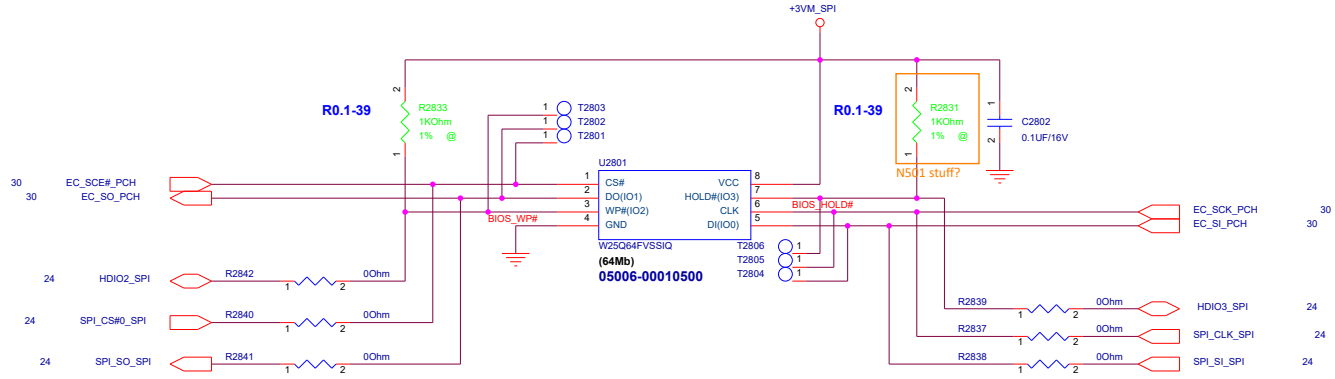
SPI Power



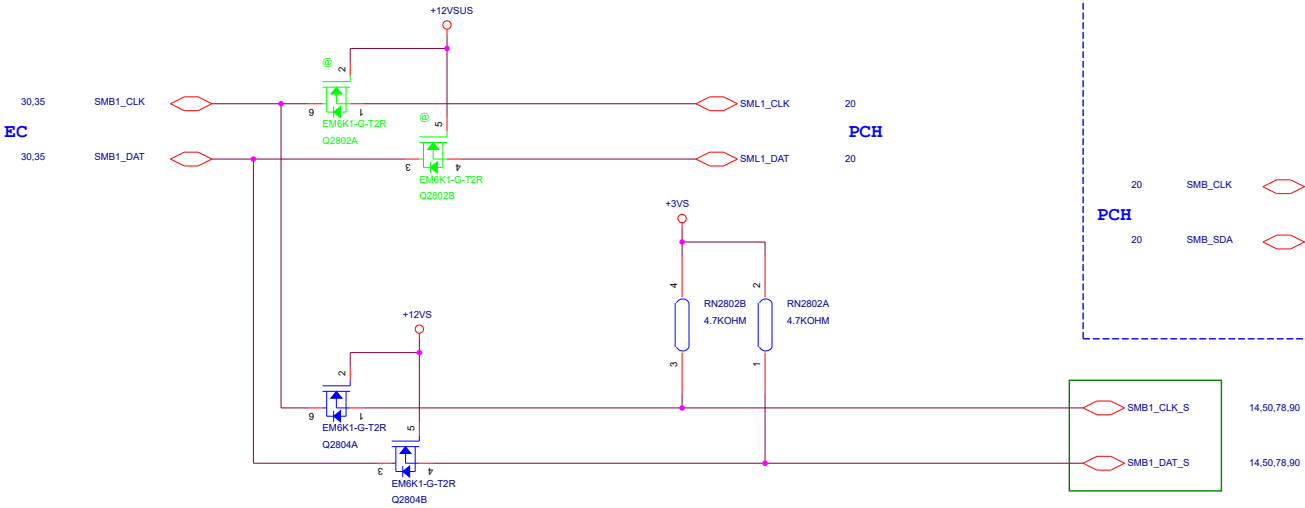


1st SPI ROM

Main: 05006-00010500 (fixed quad bit)



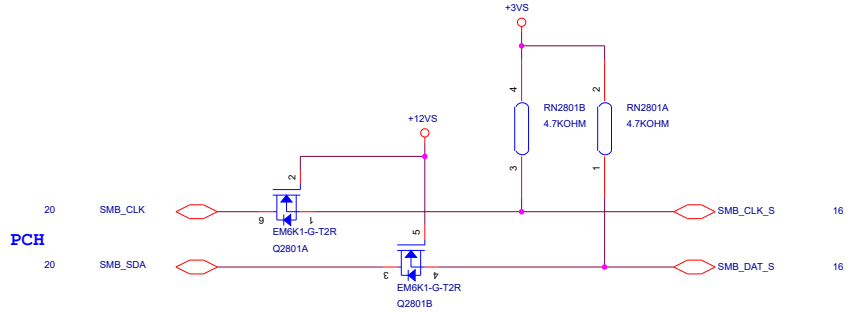
System Management Interface



R0.1-13 R1.0-01

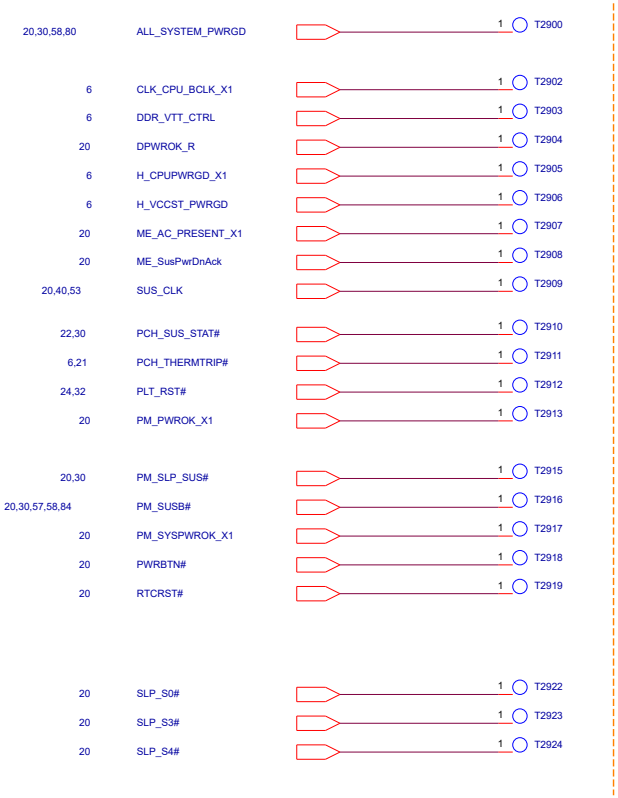
CPU,VGA Thermal Sensor
Power Thermal Sensor

SMBus Interface



ASUS	Project Name: GL502		Rev: 1.0
Title : PCH-SPI ROM,OTH			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 28 of 102		

VL1.0-09



ASUS	Project Name: GL502		Rev: 1.0
Title : PCH-XDP			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Wendell_Lo	
Date: Monday, July 25, 2016	Sheet 29 of 102		

EC 8995

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

ITE Version	ASUS P/N
IT8995VG-128/CX	06037-00050600

N key

2016.03.21 N key Design

Power

R1.0-29

PU/PD

for load code

ClickPad Schematic

2016.03.21 N key Design

Battery

Thermal sensor

2015.08.21 EMI Modify

For EMI

Close U3001

R1.0-34

R1.0-25 R1.0-38 To CC logic at p49

R1.0-41

R1.0-42

<Variant Name>

CR_KBC_IT8521

RD1_EE1

ASUSTeK COMPUTER

GL502

Monday, July 25, 2016

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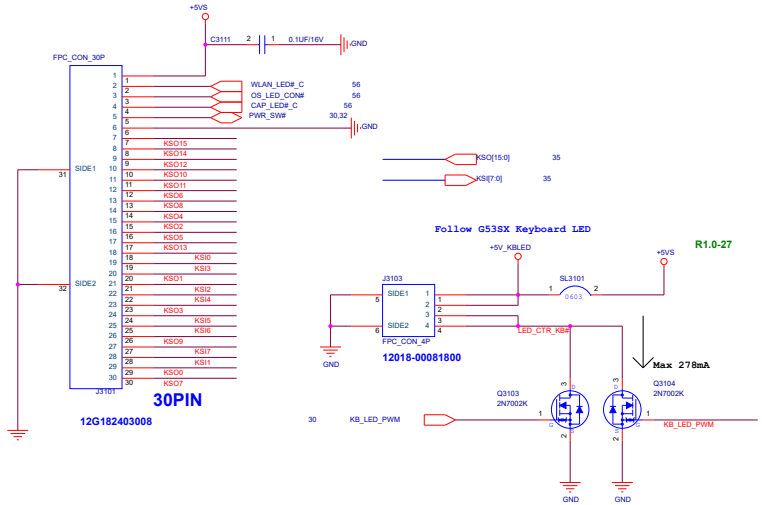
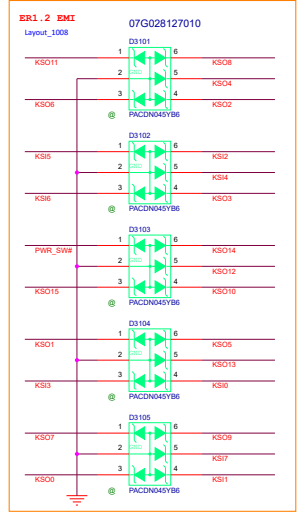
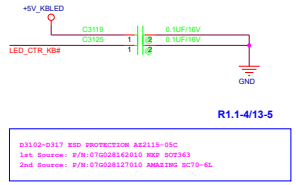
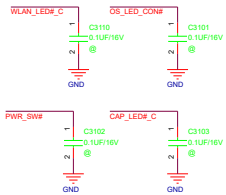
1.0

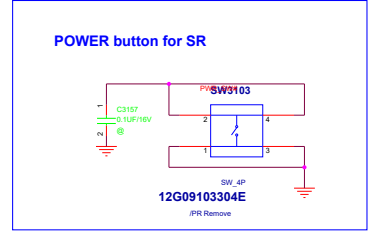
Keyboard Connector



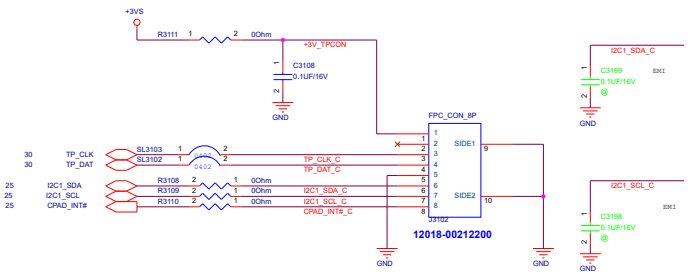




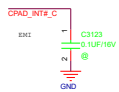


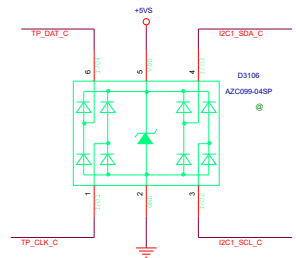


Click touch Pad Connector



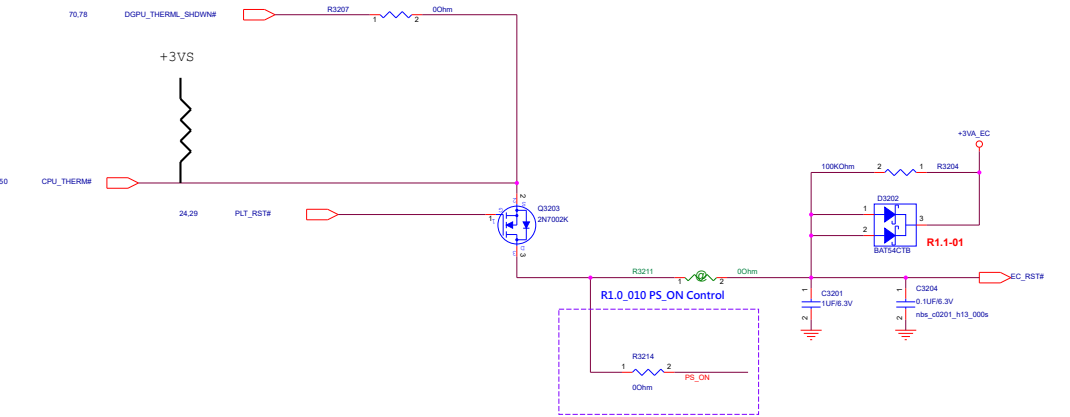
Reserved for EMI



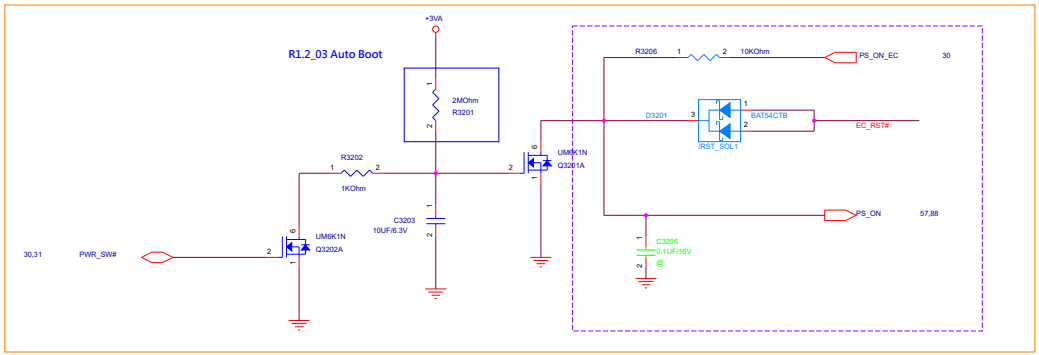


Reset Circuit

Pull up +3VSG through R7507(10kOhm=>100kOhm)
When +3VSG ready, R7507(10kOhm) and R5006(7.5kOhm) will be in parelle.
The CPU temperature point is protected ahead of time.
Increasing R7507 value can reduce to affect R5006.



Battery embedded (press pwr_sw 10sec, then reset ec)



EC power off solution:
Solution1 Mount R3206, D3201/ Unmount R3216
Solution2 Mount R3206/R3216/ Unmount D3201- for reserved 0402 footprint

R1.2-65
<Variant Name>

RST_Reset Circuit
RD1_EE1

ASUSTeK COMPUTER
B
GL502
1.0
Monday, July 25, 2016
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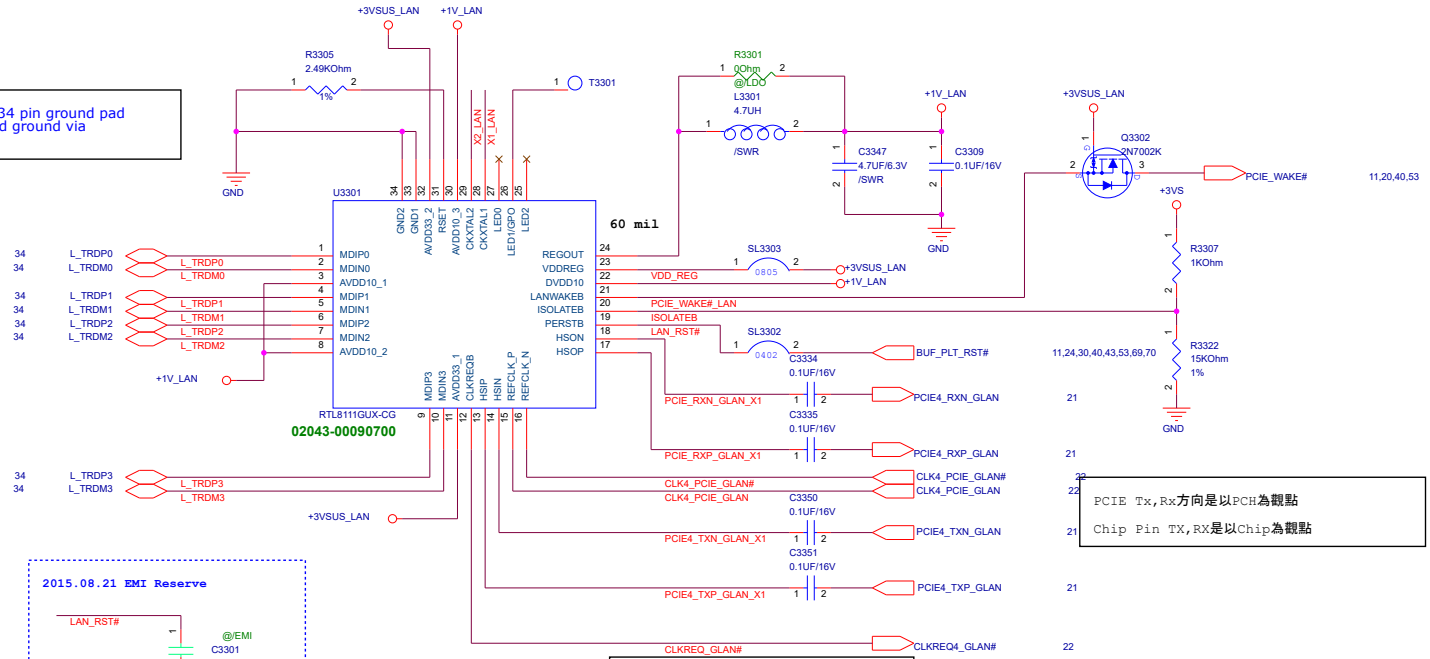
The distance from U3301.24 to L3301 within 200 mil.

The distance from L3301 to C3347 within 200 mil.

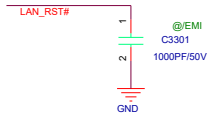
33/34 pin ground pad
need ground via



PCIE Tx,Rx方向是以PCH為觀點

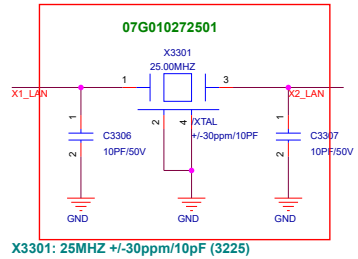
Chip Pin TX,RX是以Chip為觀點

2015.08.21 EMI Reserve



CLKREQ_GLAN#, PCIE_WAKE#
should be PU on the host side

R1.2_15 TXC Suggest

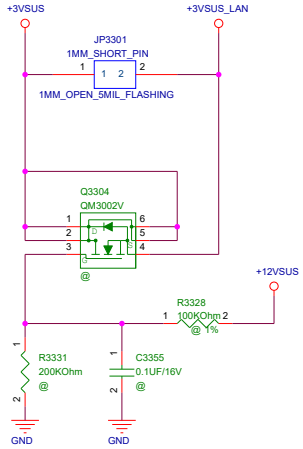


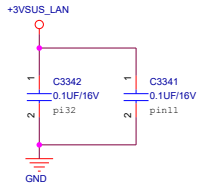
X3301: 25MHZ +/-30ppm/10pF (3225)

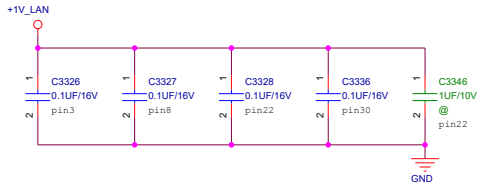
1st: P/N:07G010272501 TXC/7V25000011

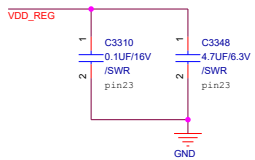
2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V_LAN raise time >1ms



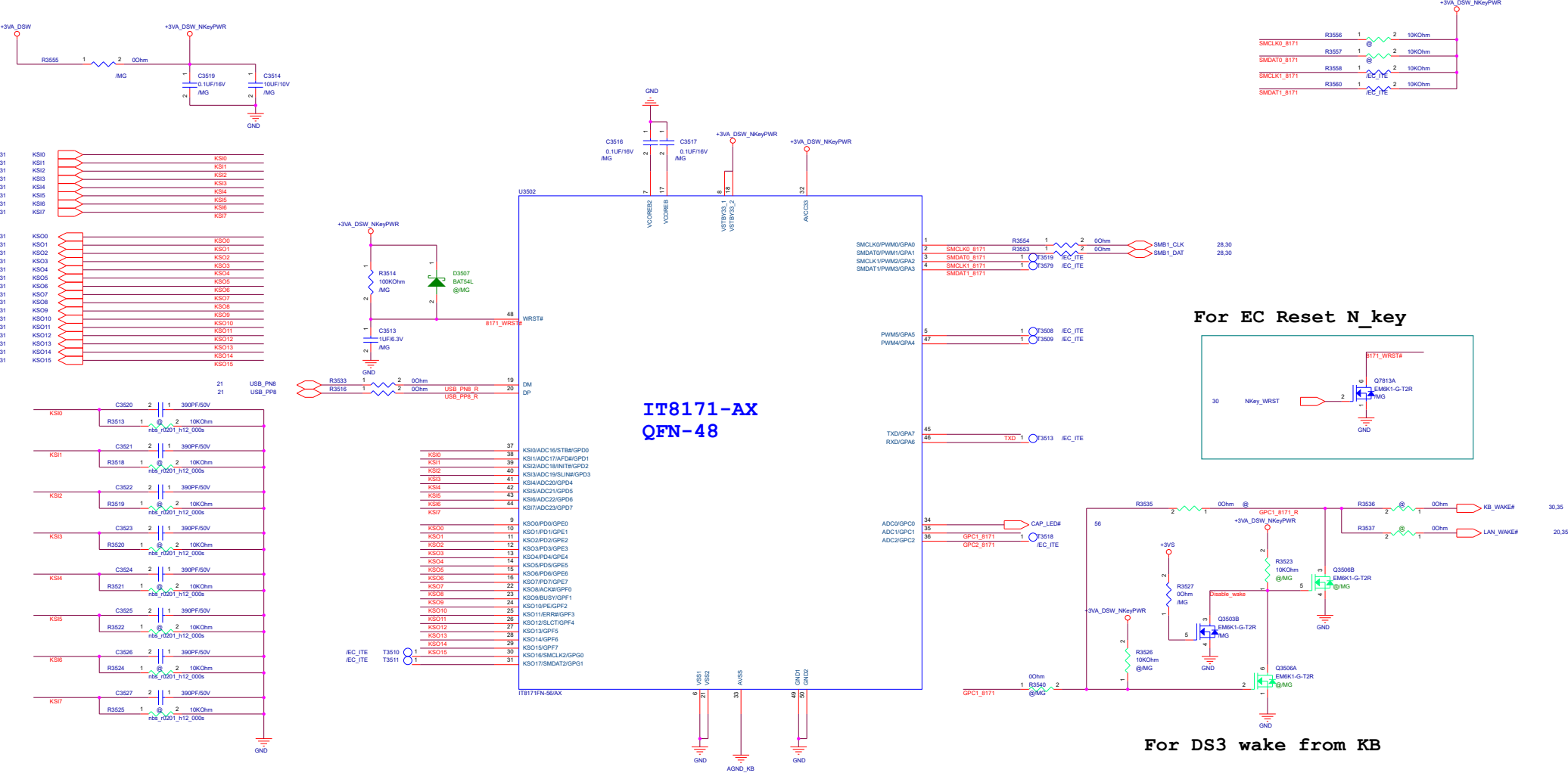


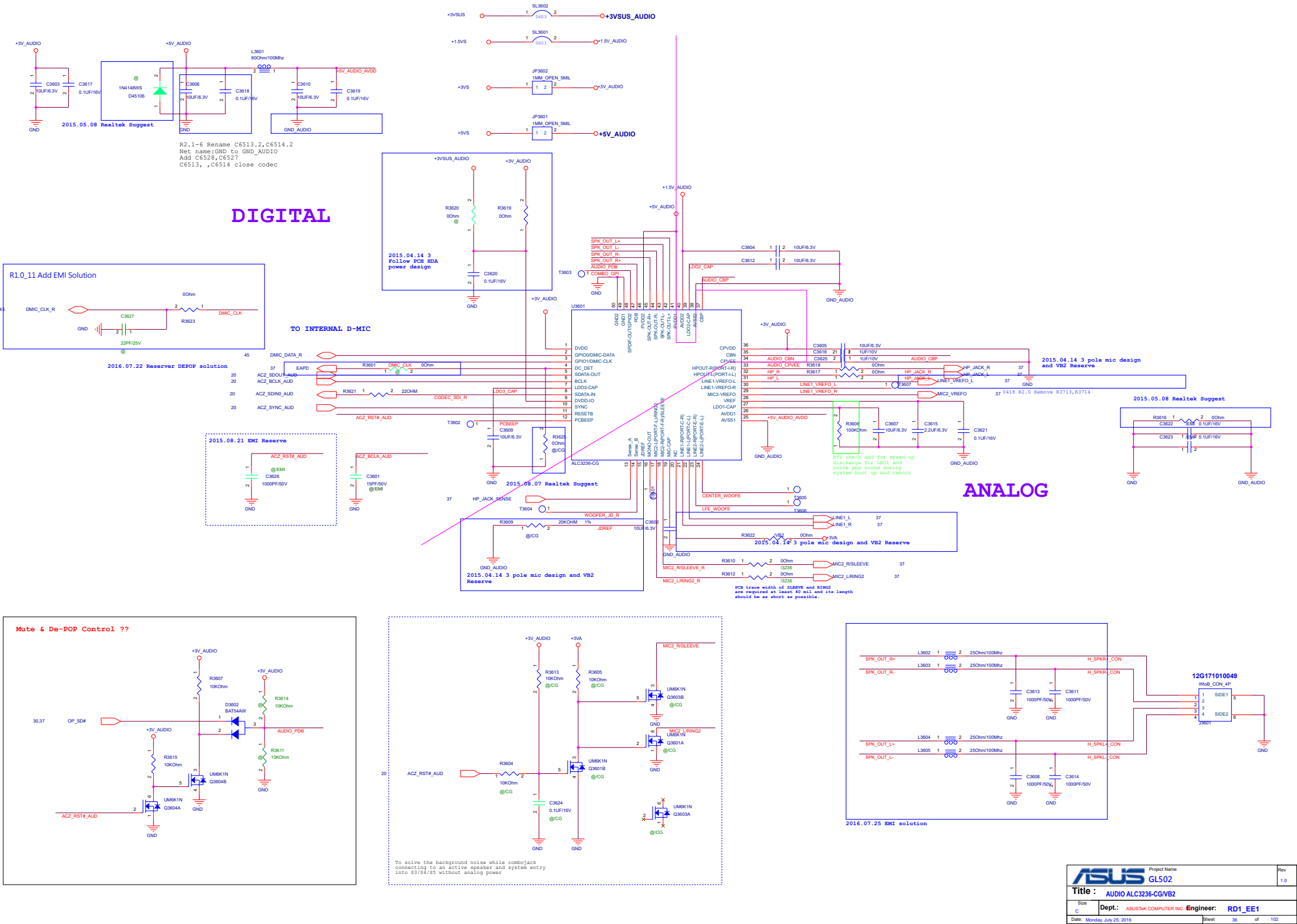




C3348, C3310 close to pin 23
reserved for SWR mode

ASUS	Project Name: GL502		Rev: 1.0
Title : LAN RTL8111GUX-CG			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD1_EE1	
Date: Monday, July 25, 2016		Sheet 33 of 102	

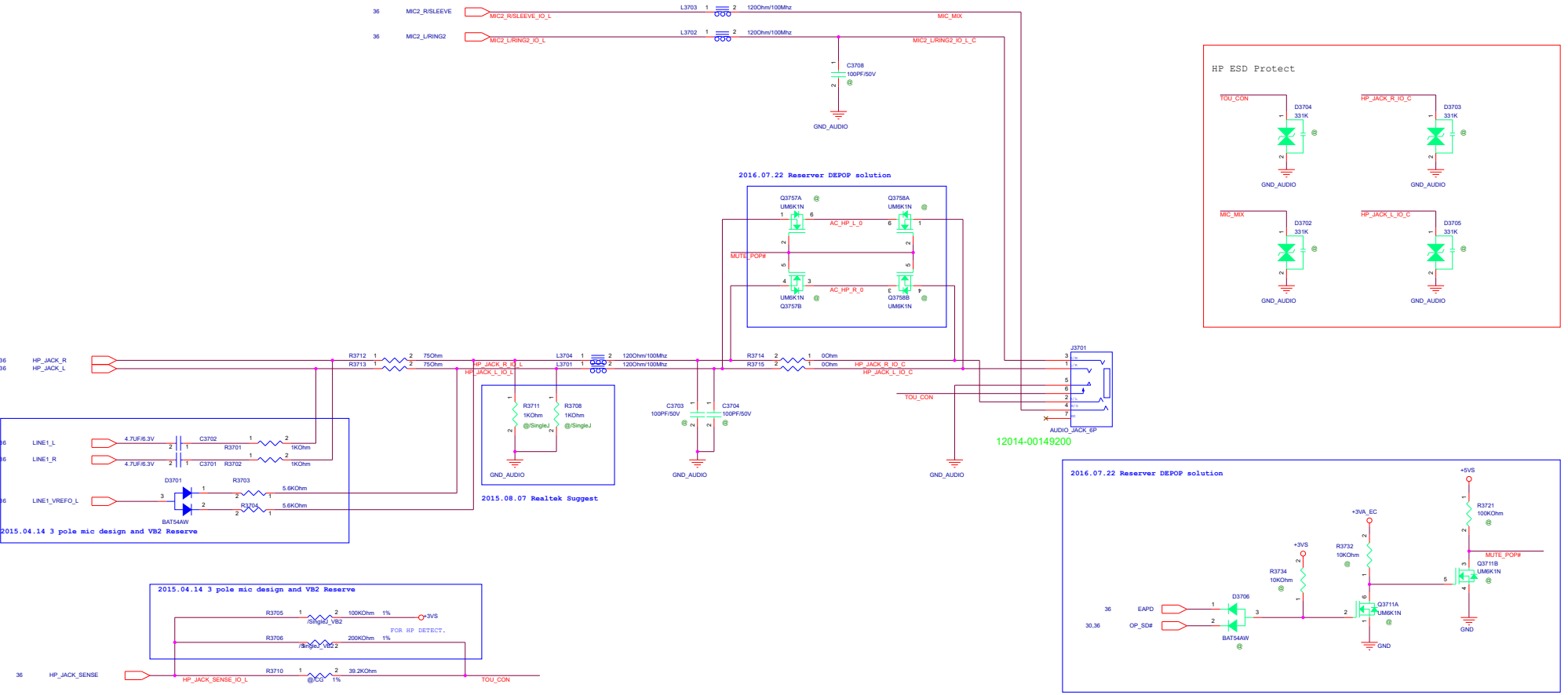

IT8171-AX
QFN-48
U3502
IT8171FN-56/AX
For EC Reset N_key
For DS3 wake from KB
For S4/S5 don't wake from KB
ITE 8171 debug con
2016.07.21 N-Key schematic update
WTOB_CON_4P
J3501
8171_WRST#
NKey_WRST
KB_WAKE#
LAN_WAKE#
1.2V_ON
Disable_wake
+3VA_DSW_NKeyPWR
+3VS
AGND_KB
GND

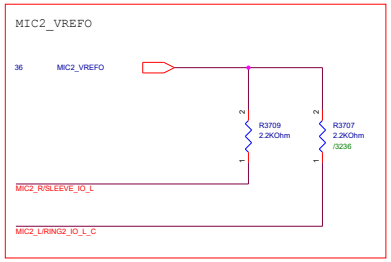


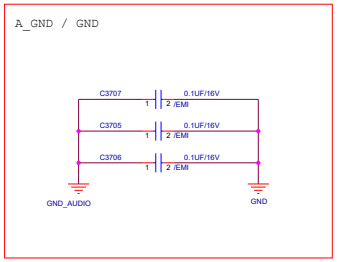
Project Name	GL502	Rev 1.0
Title :	AUDIO ALC3236-CG/VB2	
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD1_EE1
Date: Monday, July 25, 2016	Sheet 36 of 102	

Headphone&MIC

HP & MIC Connector







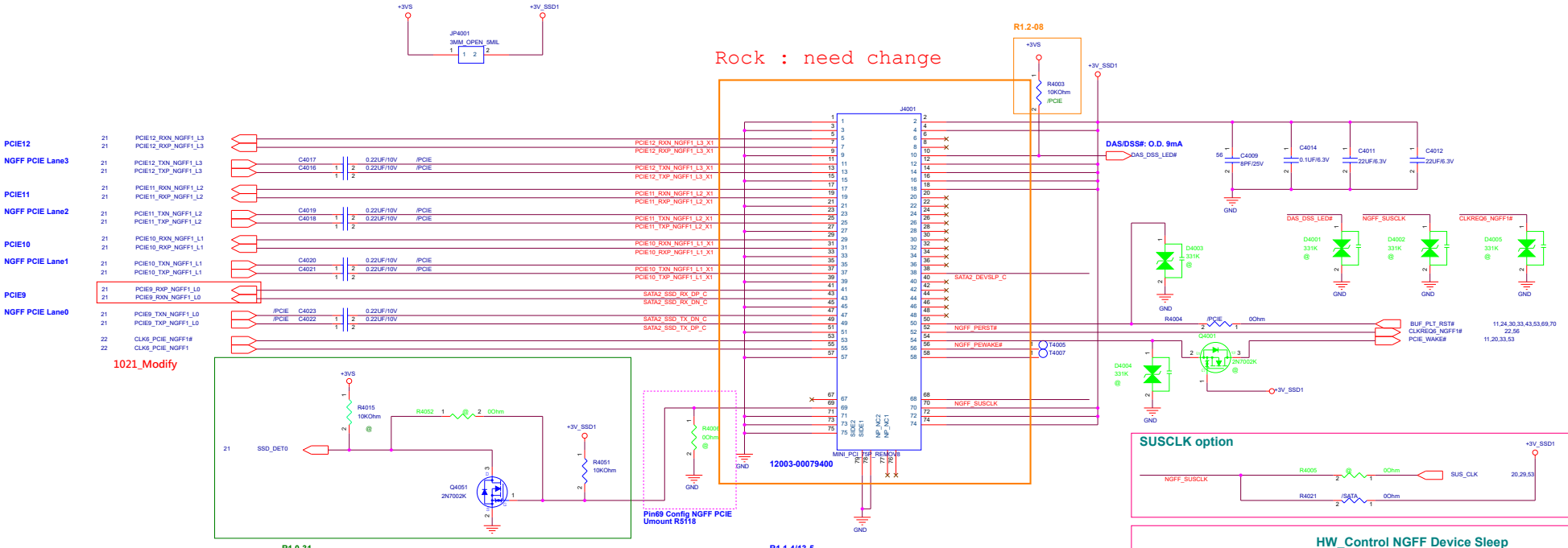
12014-00149200

ASUS	Project Name: GL502		Rev: 1.0
Title : AUDIO ALC3236-CG/VB2 Jack			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 37 of 102		

IO Board

IO Board

NGFF_SSD



SATA SSD

J4001_NGFF M-KEY PCIEx4 Connector H=3.0mm

1st Source: P/N:12003-00075100 ACES/51733-06702-012

2nd Source: P/N:12003-00075900 ARGOSY/NASM0-S6701-TPH4

3rd Source: P/N:12003-00076200 LOTES/APCI0079-P002A

4th Source: P/N:12003-00076700 DRAGONSTATE/213MAAA32FA

5th Source: P/N:12003-00076700 SINGATRON/2NF3001-012111F

SSD NUT

H4001 SMD236X236

HW Disable SSD Devslp	Mount R4002=0ohm, Unmount R4001=0ohm
HW Enable SSD Devslp	Unmount R4002=0ohm, Mount R4001=0ohm

<Variant Name>

CB_*****

RD1_EE1

ASUSTeK COMPUTER INC. NB3

A

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<Variant Name>

Card Reader-RTS5226

RD1_EE1

ASUSTeK COMPUTER INC. NB1

C

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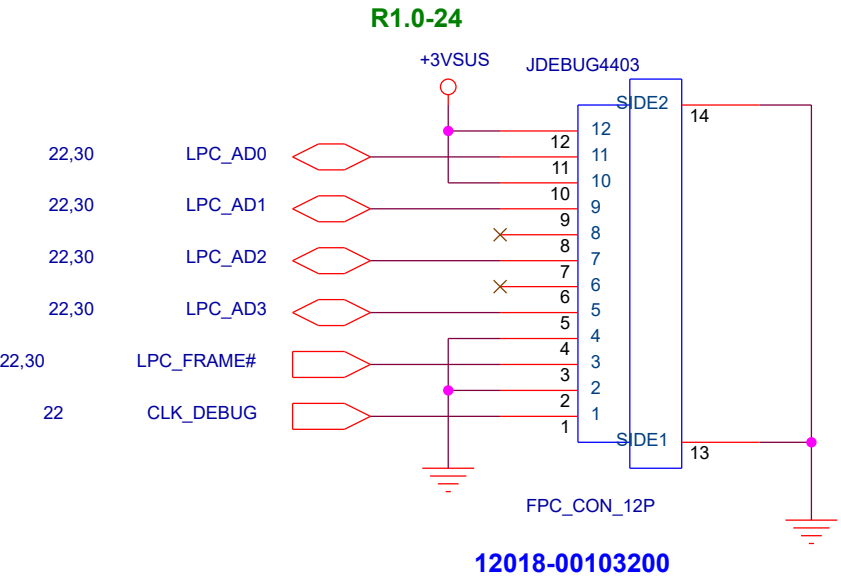
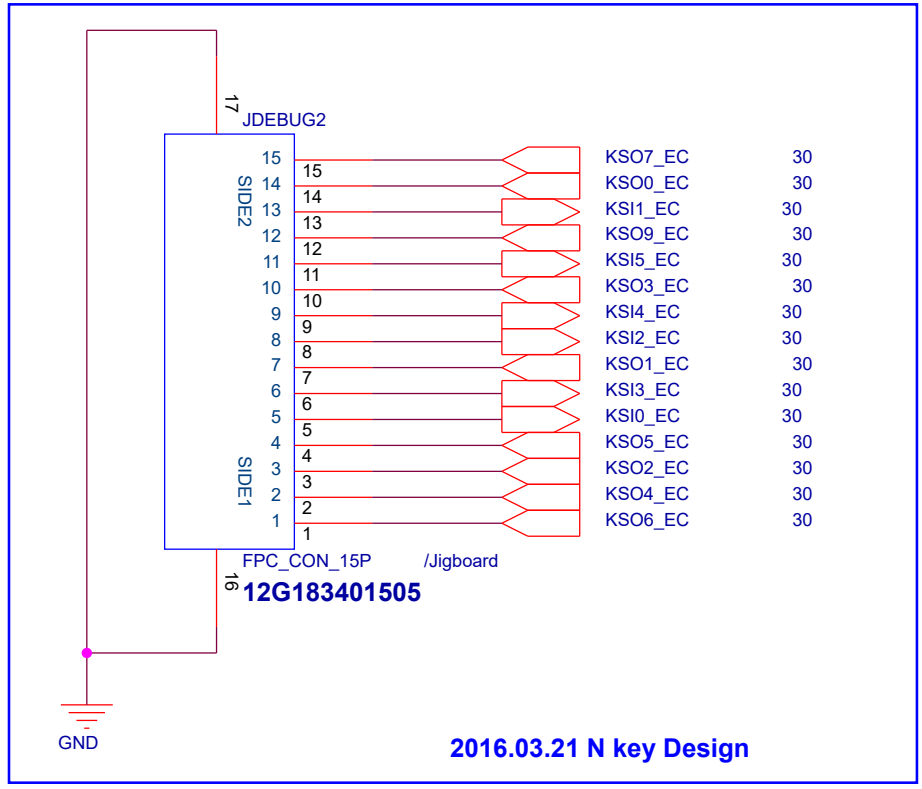
LPC Debug Port



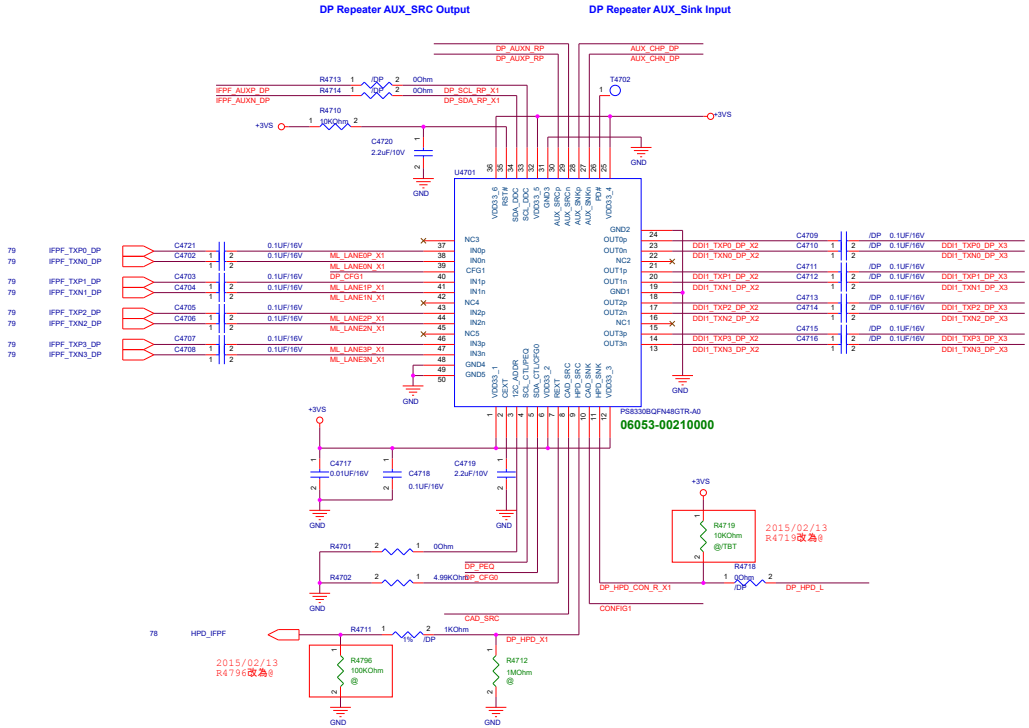


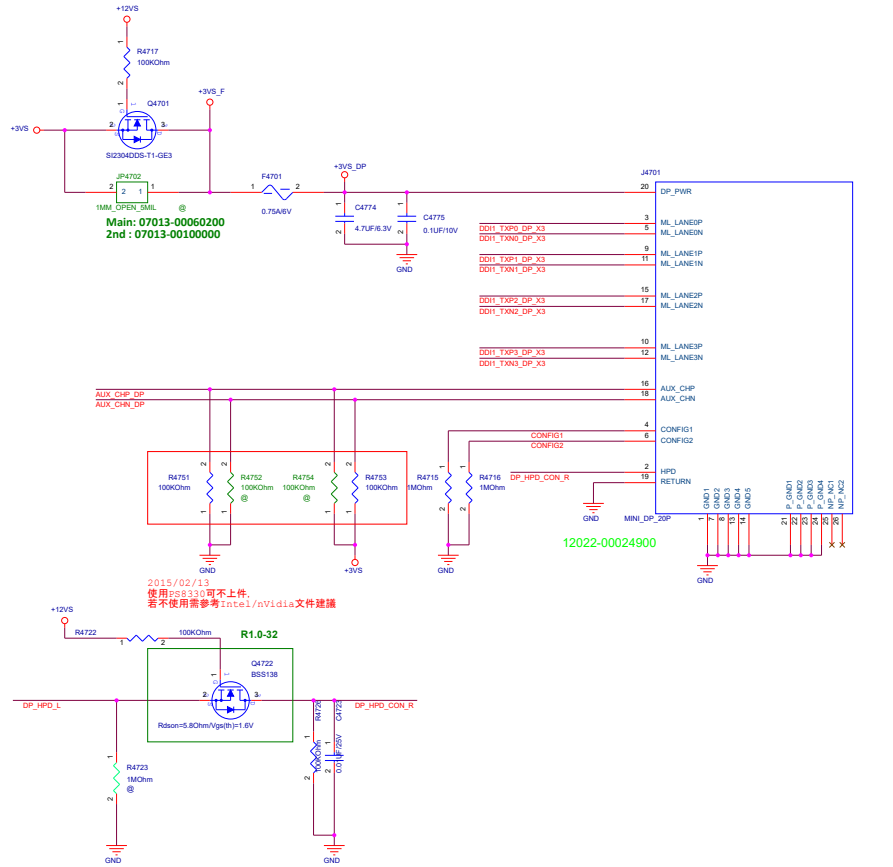
<Variant Name>

DEBUG_LPC

RD1_EE1

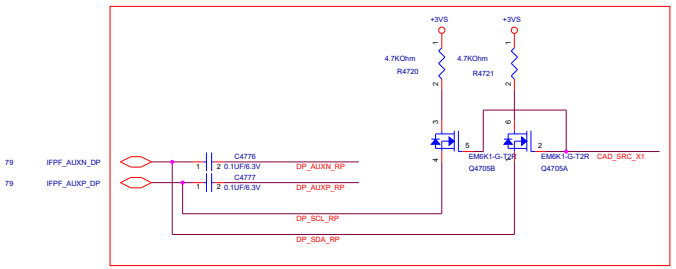
DP Repeater_PS8330B

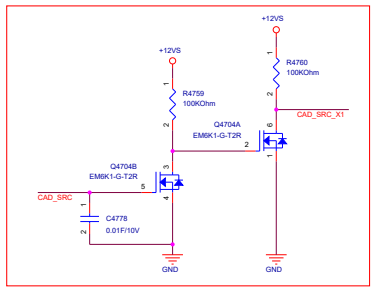


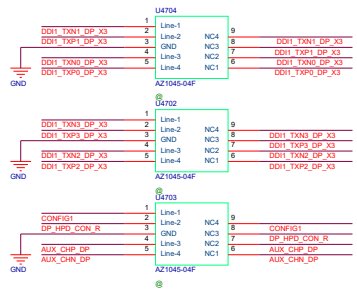


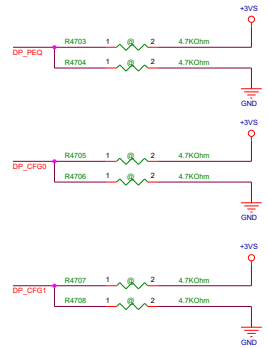
R2.0_30 reference Parade Design Circuit PS8330B

Fix MiniDP to HDMI Dongle No Display Issue









ASUS	Project Name: GL502	Rev: 1.0
Title :	Display Port Conn.	
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD1_EE1
Date: Monday, July 25, 2016	Sheet 47 of 102	

<Variant Name>

/SUS	Project Name **GL502**	Rev 1.0

Title : USB 3.1 MB Type-C

Size Custom	**Dept.:** ASUSTeK COMPUTER	**Engineer:** RD1_EE1

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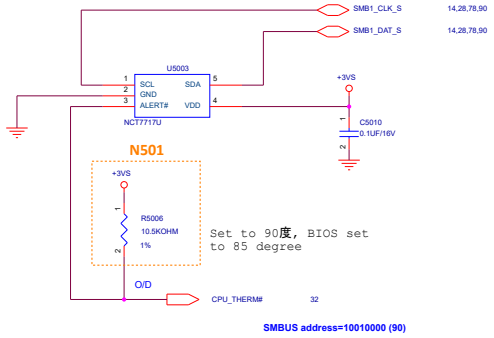
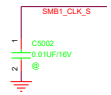
CPU Thermal Sensor

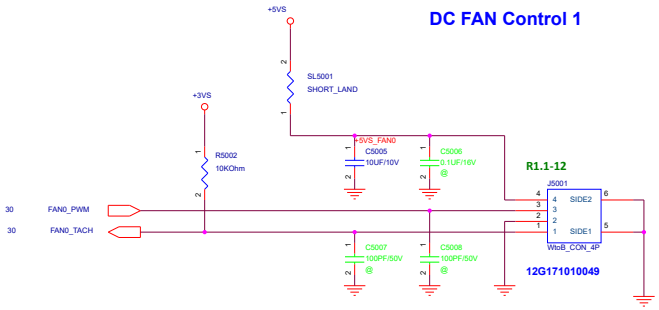


Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

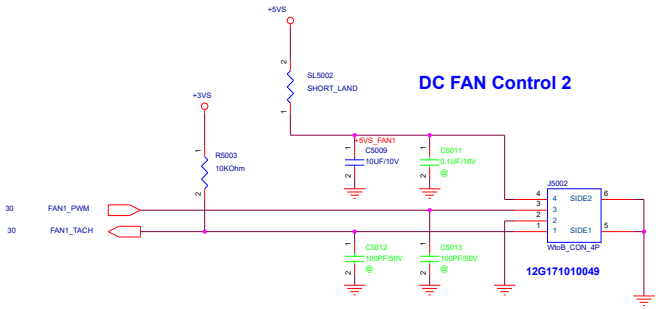
Reserve for
powr noise



DC FAN Control 1



DC FAN Control 2



<Variant Name>

FAN_Thermal Sensor & Fan

ASUSTeK COMPUTER INC. NB1

RD1_EE1

C

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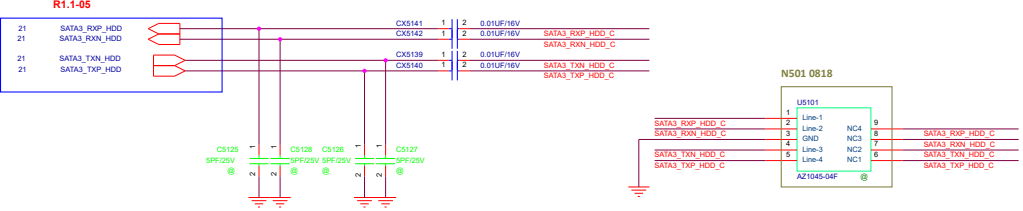
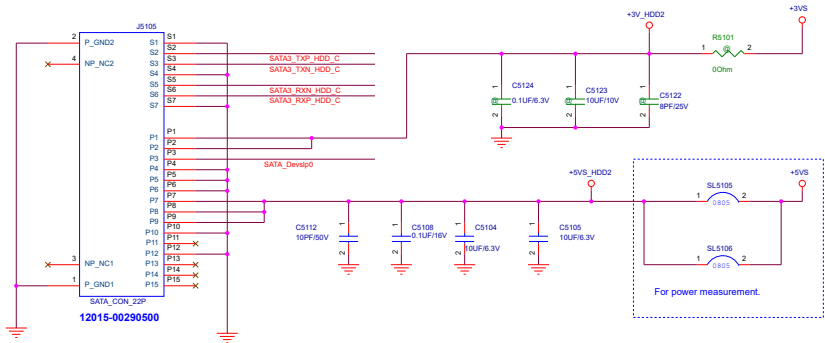
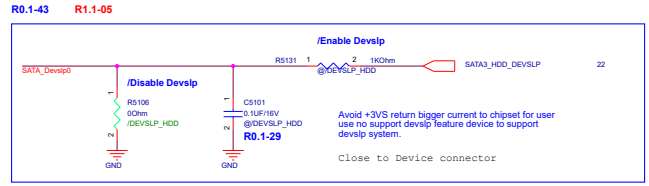
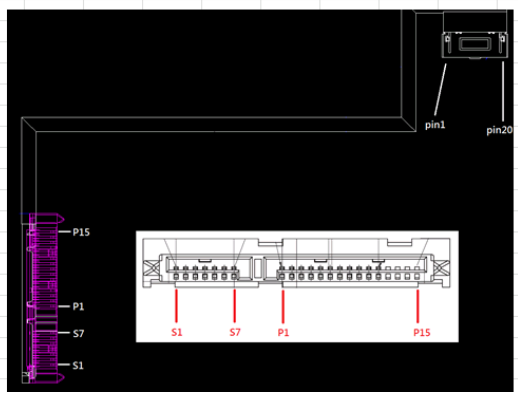






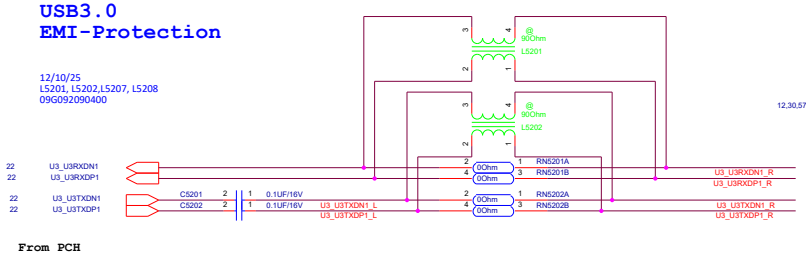
SATA Connector		
Pin	net	Note
P15	NC	
P14	NC	
P13	NC	
P12	Ground	
P11	NC	
P10	Ground	
P9	+5V	power
P8	+5V	
P7	+5V	
P6	Ground	
P5	Ground	
P4	Ground	
P3	Devslp	Impedance 50Ω
P2	+3V	power
P1	+3V	
S7	Ground	
S6	SATA_RX_P	Differential Pairs, Impedance 85Ω
S5	SATA_RX_N	Differential Pairs, Impedance 85Ω
S4	Ground	
S3	SATA_TX_N	Differential Pairs, Impedance 85Ω
S2	SATA_TX_P	Differential Pairs, Impedance 85Ω
S1	Ground	



20 pin HDD Board connector		
Pin	net	Note
pin1	Ground	
pin2	NC	
pin3	+5V	power
pin4	+5V	
pin5	+5V	
pin6	+5V	
pin7	NC	
pin8	Ground	
pin9	Devslp	Impedance 50Ω
pin10	NC	
pin11	+3V	power
pin12	+3V	
pin13	NC	
pin14	Ground	
pin15	SATA_RX_P	Differential Pairs, Impedance 85Ω
pin16	SATA_RX_N	Differential Pairs, Impedance 85Ω
pin17	Ground	
pin18	SATA_TX_N	Differential Pairs, Impedance 85Ω
pin19	SATA_TX_P	Differential Pairs, Impedance 85Ω
pin20	Ground	

USB3.0 EMI-Protection

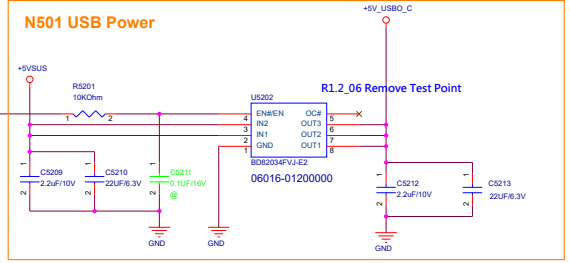
12/10/25
L5201, L5202,L5207, L5208
09G092090400



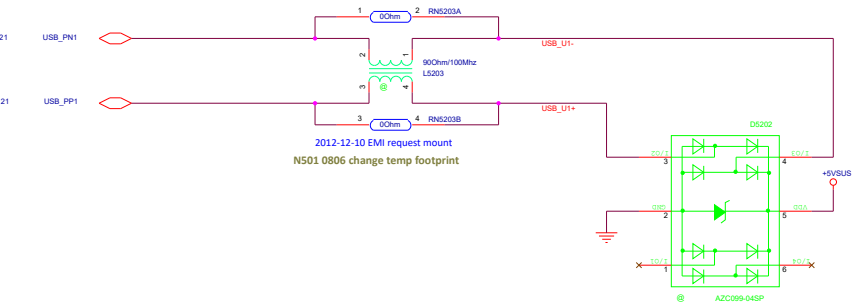
From PCH

12,30,57,63,69,88,95 SUSC_EC#

N501 USB Power

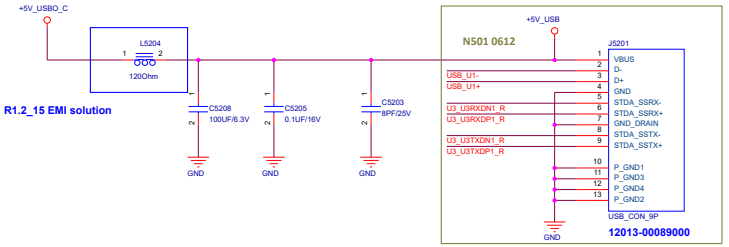


USB2.0 EMI-Protection



USB3.0_Port 0

N501 0808 change temp footprint



<Variant Name>

ASUSTeK COMPUTER INC. NB1

USB Charger
RD1_EE1

Custom GL502

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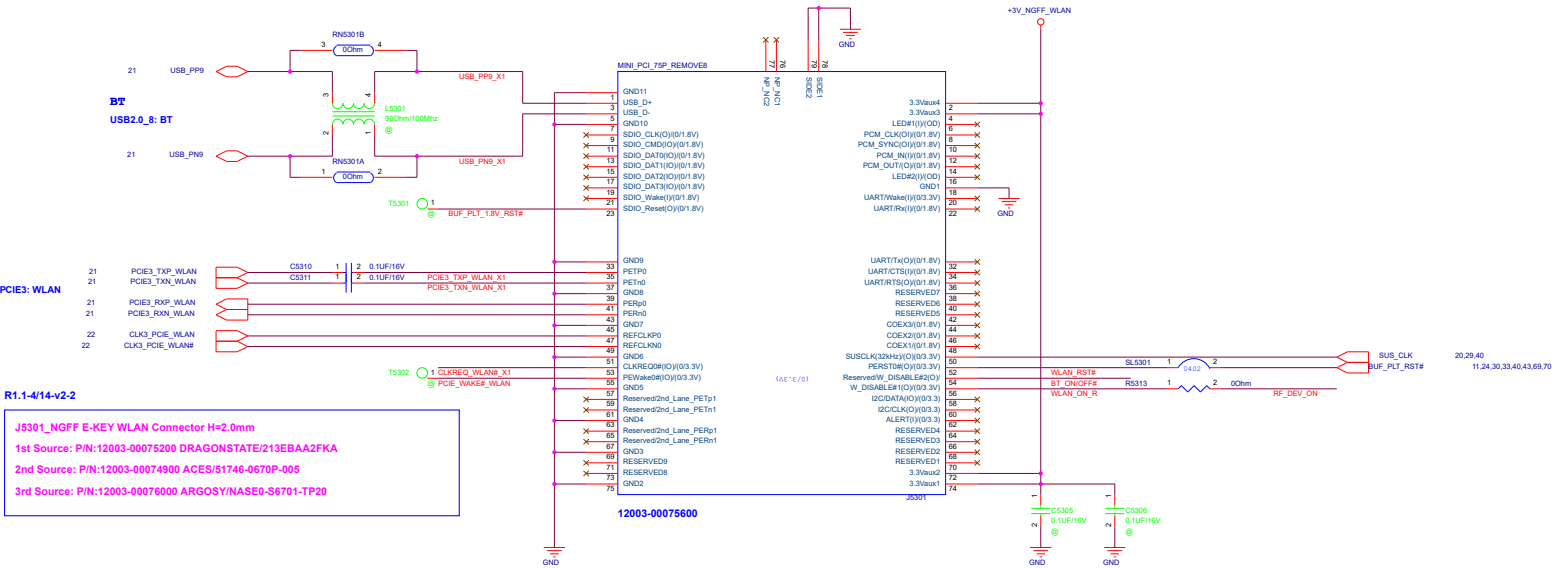
R1.1-02

NGFF M.2 TYPE_E-KEY WIFI



R1.1-4/14-v2-2

J5301_NGFF E-KEY WLAN Connector H=2.0mm

1st Source: P/N:12003-00075200 DRAGONSTATE/213EBAA2FKA

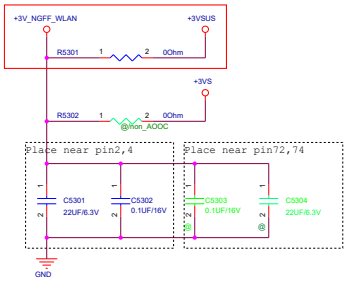
2nd Source: P/N:12003-00074900 ACES/51746-0670P-005

3rd Source: P/N:12003-00076000 ARGOSY/NASE0-S6701-TP20

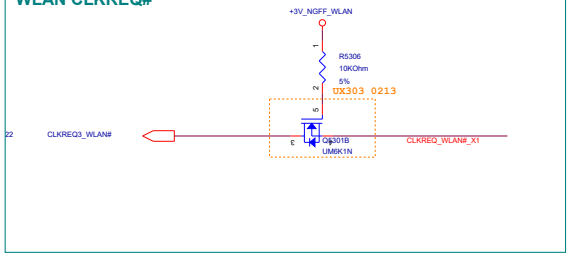
WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)

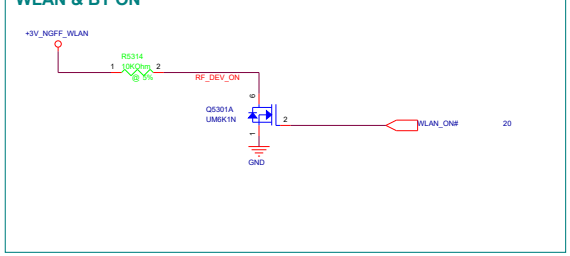
WLAN PWR to +3VSUS



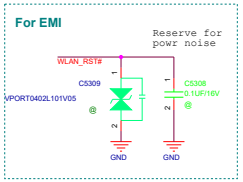
WLAN CLKREQ#



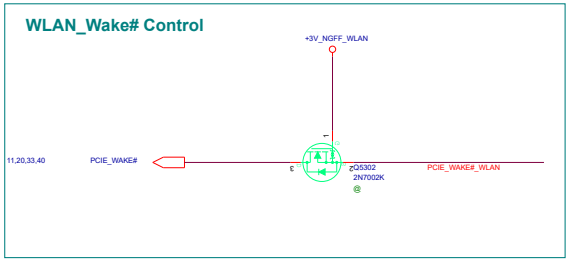
WLAN & BT ON



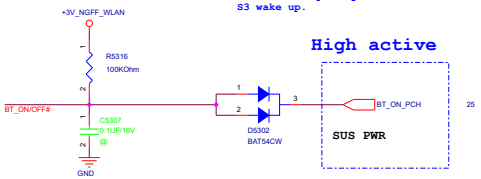
For EMI



WLAN_Wake# Control



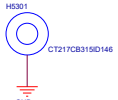
To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.



Project which use the combo card schematic should make sure that BT_ON signal can't be High at S3/S4/S5 state to prevent leakage

74	3.3Vaux	GND	75
72	3.3Vaux	RESERVED	73
70	RESERVED	RESERVED	71
68	RESERVED	GND	69
66	RESERVED	Reserved/2nd Lane PERn1	67
64	GPIO0 NFC Reset# (MGPIO7)(O)(0/3.3V)	Reserved/2nd Lane PERp1	65
62	NFC I2C IRQ (MGPIO5)(I)(0/3.3)	GND	63
60	NFC I2C SM CLK (O)(0/3.3)	Reserved/2nd Lane PETn1	61
58	NFC I2C SM DATA (IO)(0/3.3)	Reserved/2nd Lane PETp1	59
56	W_DISABLE#1 (O)(0/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX1 (?)(0/1.8V)	REFCLKN0	49
46	COEX2(?)(0/1.8V)	REFCLKP0	47
44	COEX3(?)(0/1.8V)	GND	45
42	CLink CLK	PERn0	43
40	CLink DATA	PERp0	41
38	CLink RESET (O)(0/3.3V)	GND	39
36	UART CTS (O)(0/1.8V)	PETn0	37
34	UART RTS (I)(0/1.8V)	PETp0	35
32	UART Tx (O)(0/1.8V)	GND	33
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
22	UART Rx (I)(0/1.8V)	SDIO Reset[O](0/1.8V)	23
20	UART Wake (I)(0/3.3V)	SDIO Wake(I)(0/1.8V)	21
18	GND	SDIO DAT3(IO)(0/1.8V)	19
16	LED#2 (I)(OD)	SDIO DAT2(IO)(0/1.8V)	17
14	PCM_OUT (I)(0/1.8V)	SDIO DAT1(IO)(0/1.8V)	15
12	PCM_IN (O)(0/1.8V)	SDIO DAT0(IO)(0/1.8V)	13
10	PCM_SYNC (O)(0/1.8V)	SDIO CMD(IO)(0/1.8V)	11
8	PCM_CLK (O)(0/1.8V)	SDIO CLK(O)(0/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3Vaux	USB_D-	5
2	3.3Vaux	USB_D+	3
		GND	1

NGFF NUT



13020-00780900

<Variant Name>

WiFi/WiMax

RD1_EE1

<Variant Name>

USB3_*****

RD1_EE1

ASUSTeK COMPUTER INC

C

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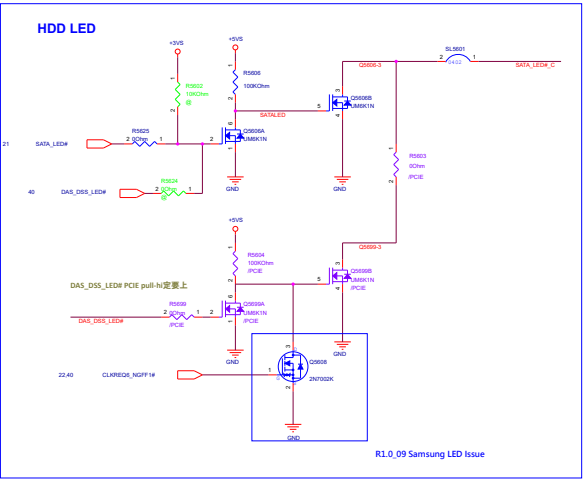
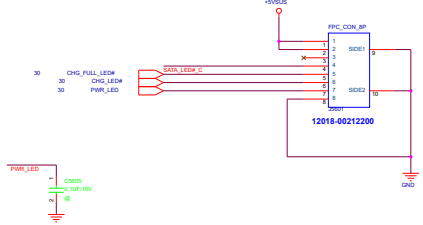
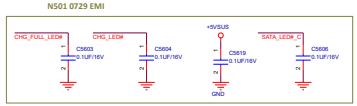
IO Board

2014/05/29 Add HDD & SSD LED control circuit.

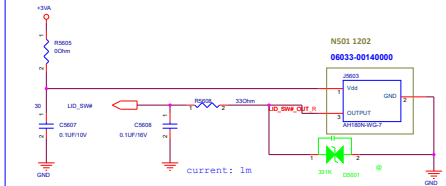
HDD LED



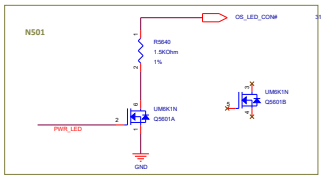




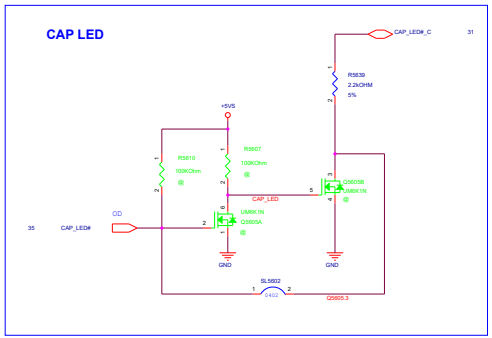
HALL SENSOR
06033-00140000



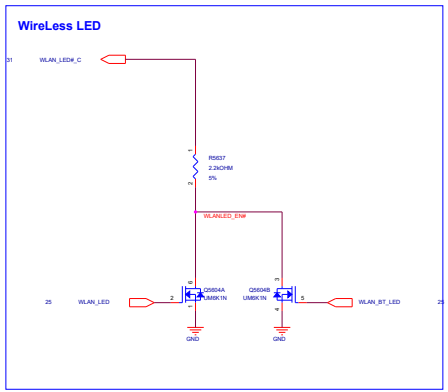
OS LED



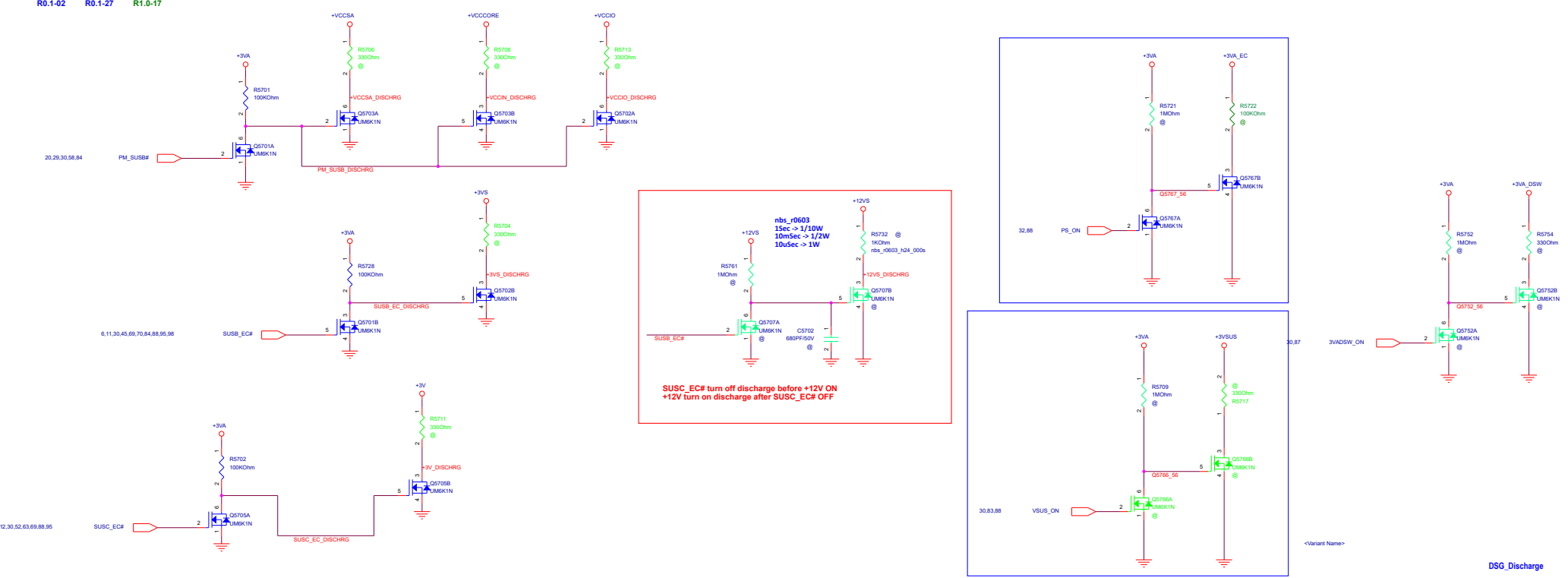
CAP LED



WireLess LED



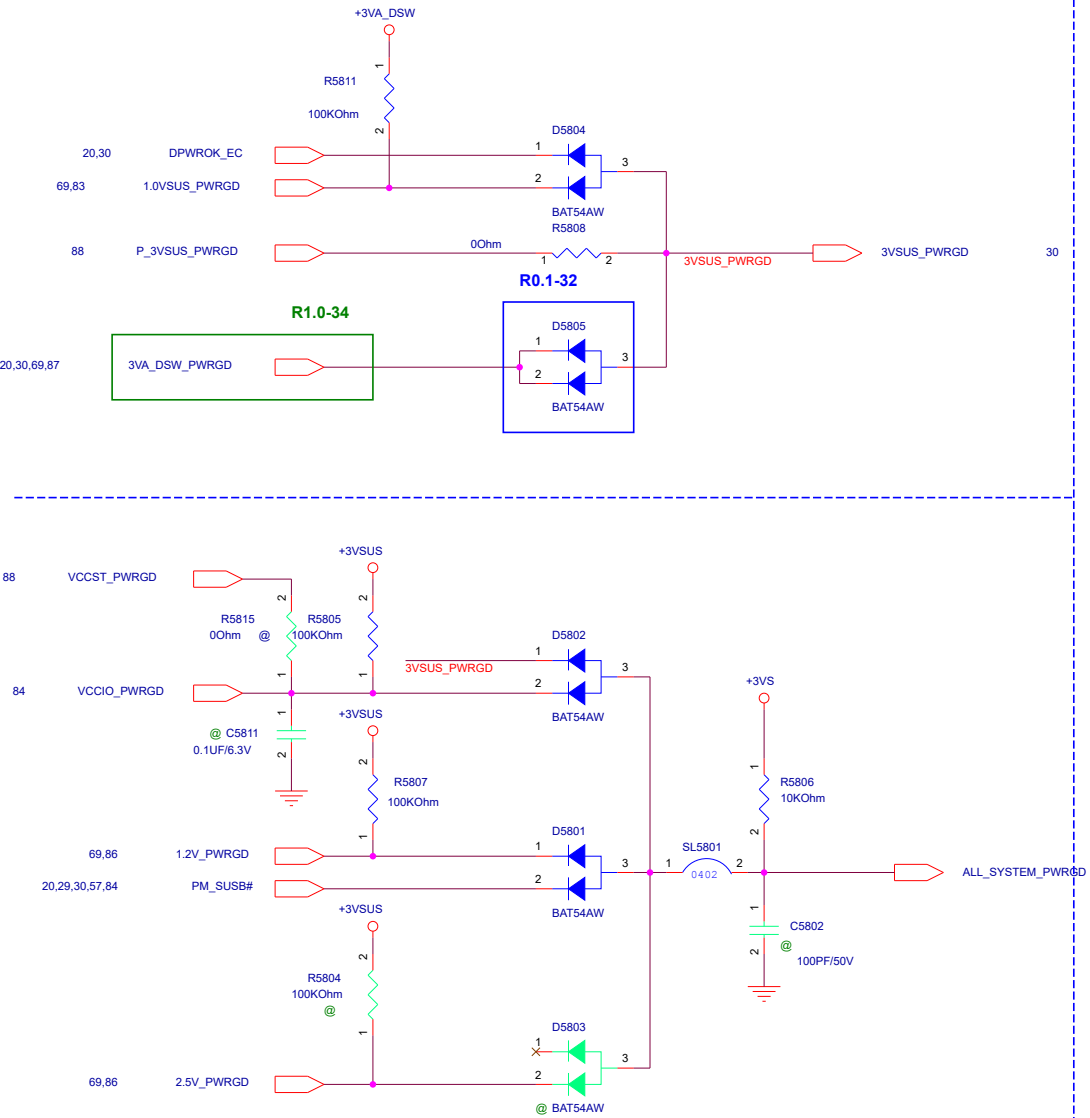
R0.1-02 R0.1-27 R1.0-17

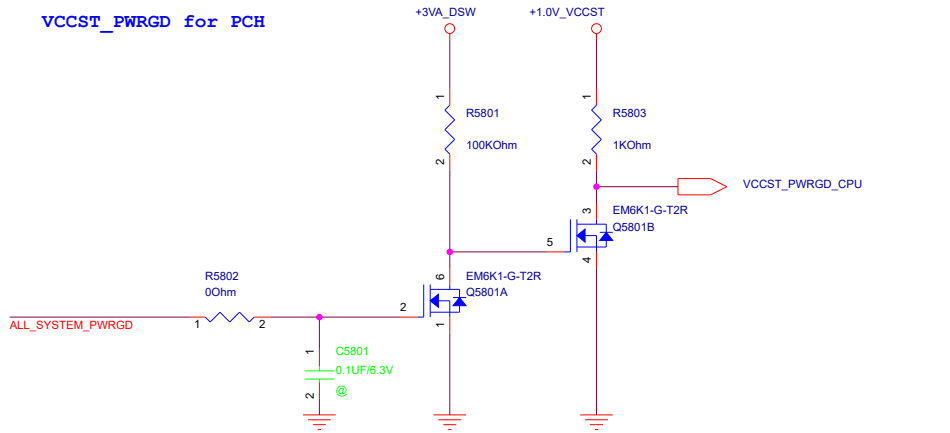


<Variant Name>

DSG_Discharge

RD1_EE1





<Variant Name>

ASUSTeK COMPUTER

Power Protect

RD1_EE1

Custom

GL502

1.0

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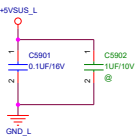
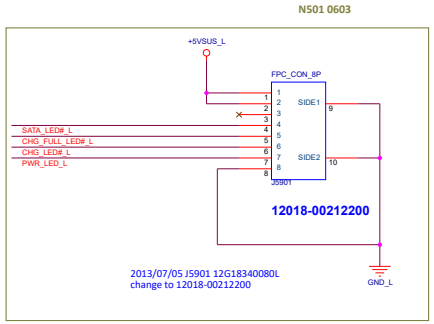
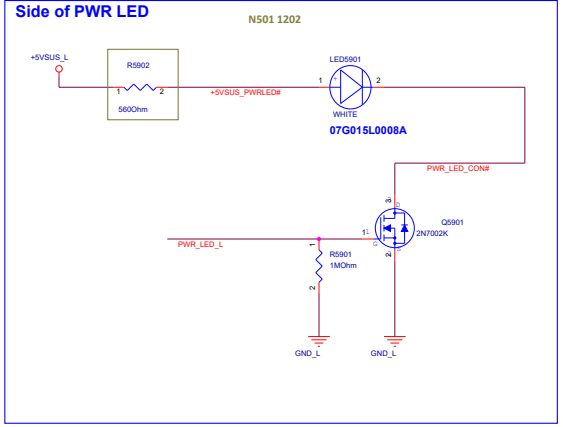
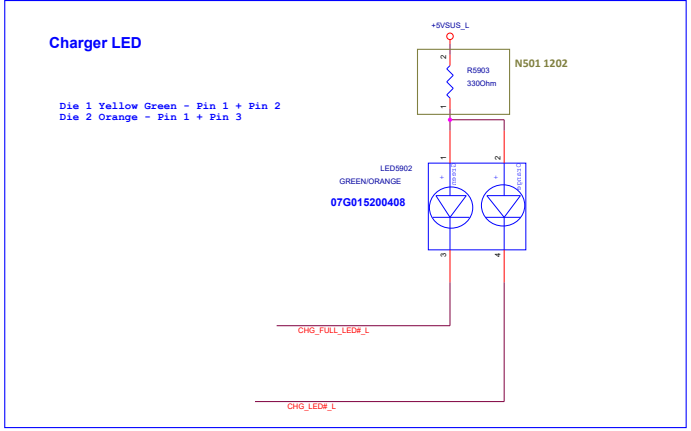
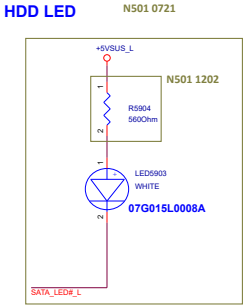
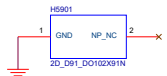


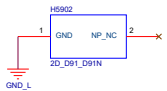


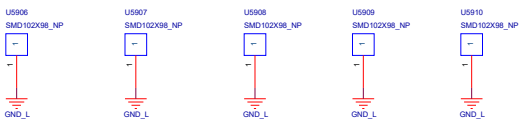


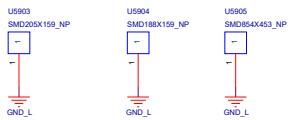


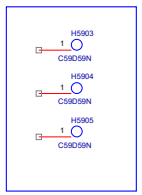




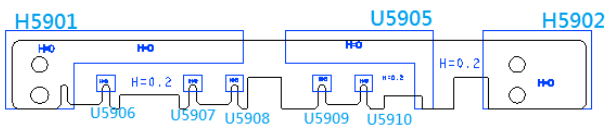


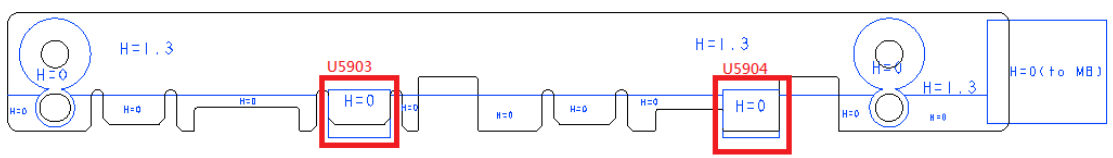




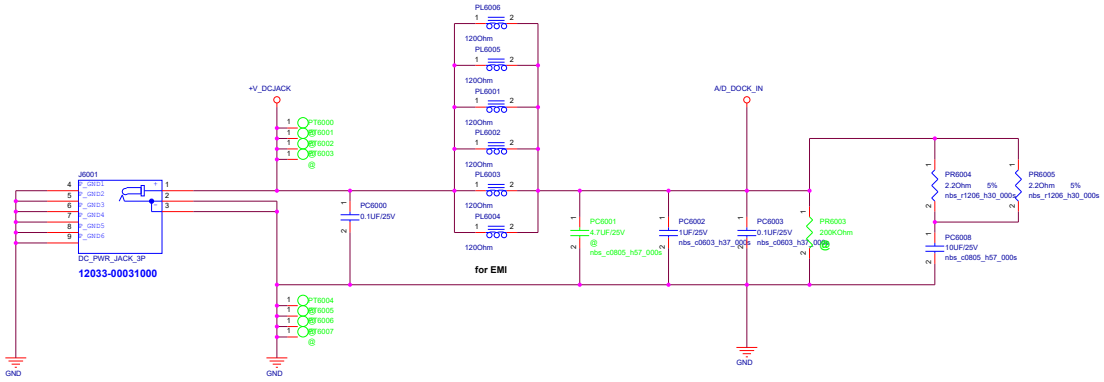


2015.11.05 add by ME

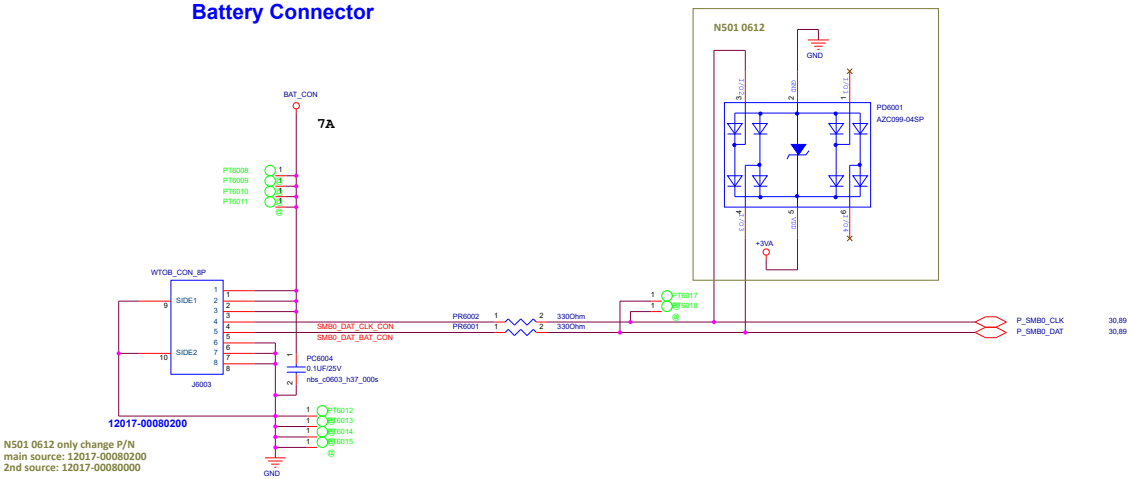




DC-IN Connector



Battery Connector



N501 0612 only change P/N
main source: 12017-00080200
2nd source: 12017-00080000

DC & BAT IN

<Variant Name>

ASUSTeK COMPUTER INC. NB1

BT_Bluetooth

RD1_EE1

A

GL502

1.0

Monday, July 25, 2016

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<Variant Name>

I/O board(1-1)_CR_RTS5139

RD1_EE1

ASUSTeK COMPUTER INC. NB3

C

GL502

1.0

Monday, July 25, 2016

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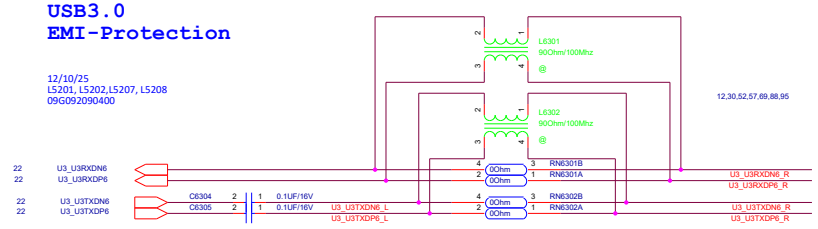
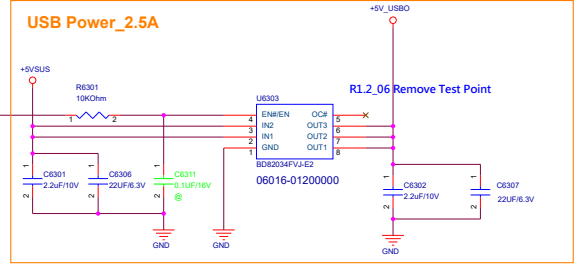
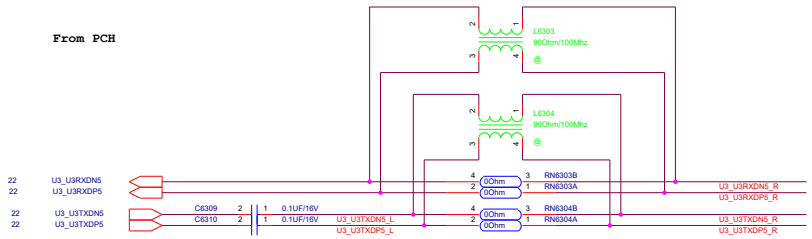
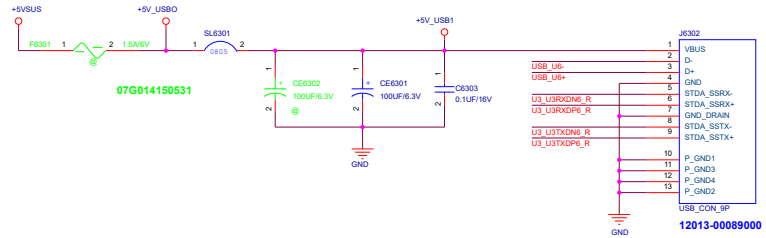
USB3.0 EMI-Protection

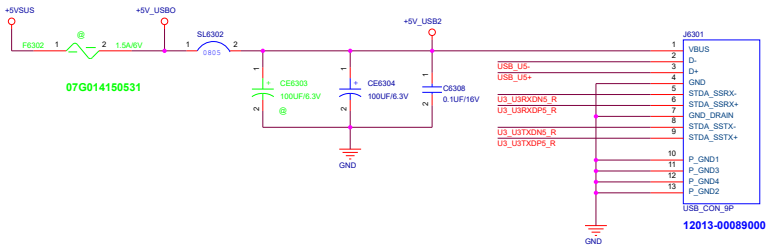
12/10/25
L5201, L5202,L5207, L5208
09G092090400





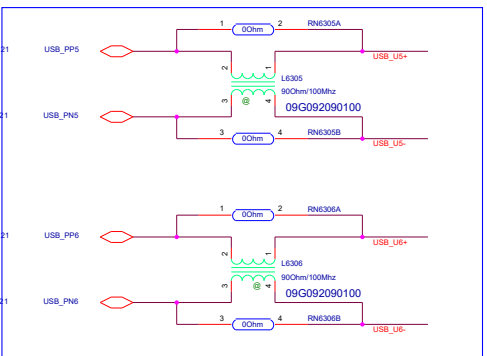






USB2.0 EMI-Protection

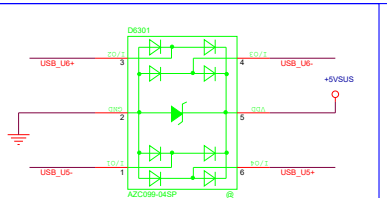
R1.1-4/13-5



L5204 & L5206 C.M. CHOKE(0805)90 OHM/330mA
1st Source: P/N:09G09209011D INPAQ/MCM2012D900FBE
2nd Source: P/N:09G092090300 TAI-TECH/WCM2012F2SF-900T04
3rd Source: P/N:09G092090110 MURATA/DLW21SN900SQ2L
4th Source: P/N:09G092090107 CHILISIN/CMM21T-900M-S
5th Source: P/N:09G092090100 MURATA/DLW21HN900SQ2L

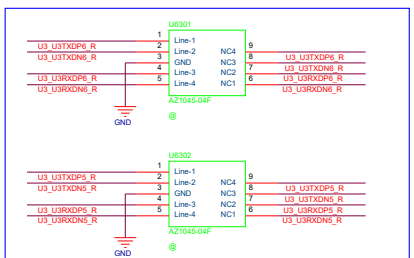
R1.1-4/13-5

D5201 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



USB3.0/USB 2.0 ESD-Protection

R1.1-4/13-5



U5201 & U5203 ESD PROTECTION
1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

<Variant Name>

USB Port
RD1_EE1

ASUSTeK COMPUTER INC. NB1

C GL502

Monday, July 25, 2016 63 1.0

<Variant Name>

PWR_ BAT_CON & GAUGE

ASUSTek Computer INC

RD1_EE1

C

GL502

1.0

Monday, July 25, 2016

64

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<Variant Name>

PWR_ BAT_CON & GAUGE

RD1_EE1

ASUSTek Computer INC

C

GL502

1.0

Monday, July 25, 2016

<Variant Name>

EC_IT8569

RD1_EE1

ASUSTeK COMPUTER INC. EPAD

GL502

Custom

1.0

Monday, July 25, 2016

66

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shielding case screw hole

PCH NUT

2016.05.06
delete H6711,H6712

H6731 2D_D94 GND GND
H6732 2D_D110_DO94X106N GND GND
H6735 2D_D94_D94N GND GND
H6736 2D_D110_DO94X106 GND GND
H6744 CT354CB315D94 GND
H6742 CT256CB315I114D94 GND
H6741 CT256CB315I114D94 GND
H6743 CT256CB315I114D94 GND

H6733 P_GND NP_NC1 NP_NC2 NP_NC3 NP_NC4 NP_NC5 NP_NC6 NP_NC7 NP_NC8 NP_NC9 NP_NC10 NP_NC11 NP_NC12 NP_NC13 14D_D110_C31D31N GND
2016.05.06 update
H6734 RT591X512CB315D110 GND

2016.05.06 update
H6760 C354D94 GND
H6745 CT354CRB315x335D94 GND

FAN NUT
H6705 CT217CB176D146
H6707 CT217CB176D146
H6708 CT217CB176D146
H6709 CT217CB176D146
H6710 CT217CB176D146

GPU bracket tooling hole

R1.2_18 Remove GPU Breaket

CPU skrew hole

CPU NUT
H6748 CT217CB176D146 GND
H6749 CT217CB176D146 GND
H6750 CT217CB176D146 GND
H6751 CT217CB176D146 GND

GPU NUT 2016.05.06 update
H6752 CT236CB176D146 GND
H6753 CT236CB176D146 GND
H6754 CT236CB176D146 GND
H6755 CT236CB176D146 GND

H6721 P_GND1 P_GND2 P_GND3 P_GND4 P_GND5 P_GND6 P_NGD7 7D_D104_D110_D114 GND
H6728 P_GND1 P_GND2 P_GND3 P_GND4 P_GND5 P_GND6 P_NGD7 7D_D114_D104_D110 GND
H6722 OT111X99BIDO91X79
H6723 OT111X99BIDO91X79
H6756 OB169X94DO130X55
H6757 OB169X94DO130X55

<COMPONMENT BOT>

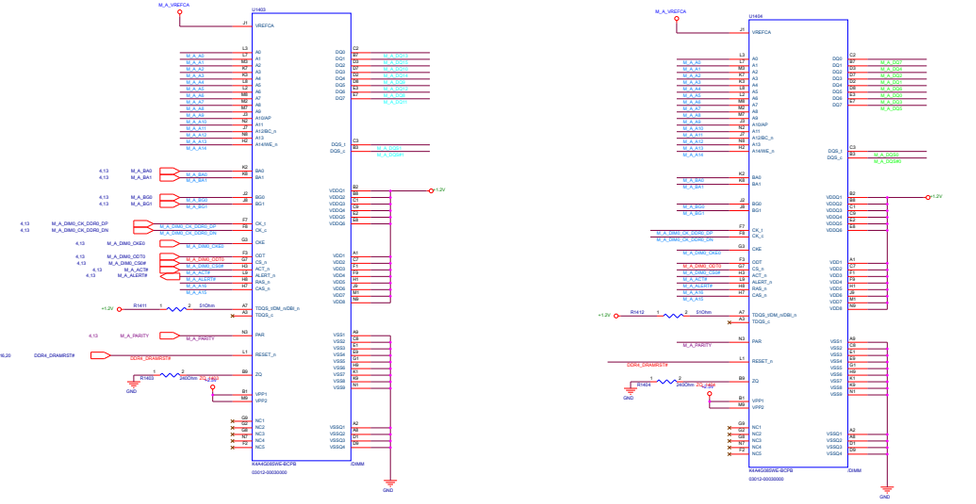
H6770 H6771 H6721 H6722 H6707 H6761 H6723 H6731 H6708 H6741 H4001 H6732 H6760 H6745 H6733 H6734 H6752 H6753 H6748 H6749 H6724 H6725 H6717 H6718 H6751 H6762 H6706 H6742 H6719 H6750 H6720 H6754 H6755 H6763 H6726 H6727 H6704 H6703 H6702 H6701 H6705 H6743 H6712 H6711 H6746 H6747 H6728 H6710 H5301 H6735 H6709 H6744 H6736

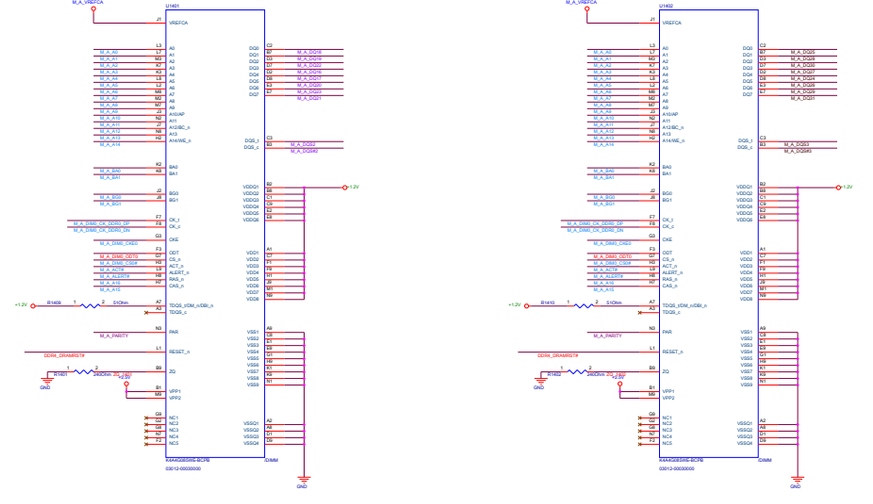
H6761 O79X67DO79X67N
H6764 O79X67DO79X67N
H6763 C67D67N
H6746 CT354CRB315x335D94 GND
H6747 CT354CRB315x335D94 GND

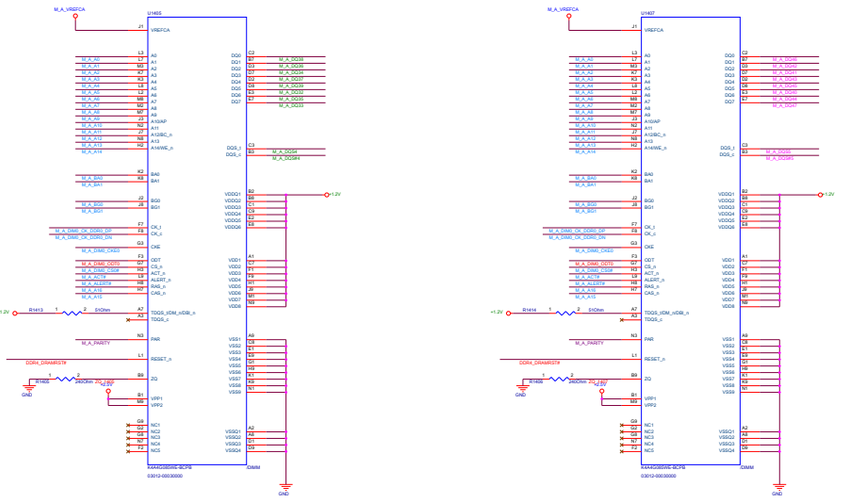
2016.05.06
delete H6762

<Variant Name>

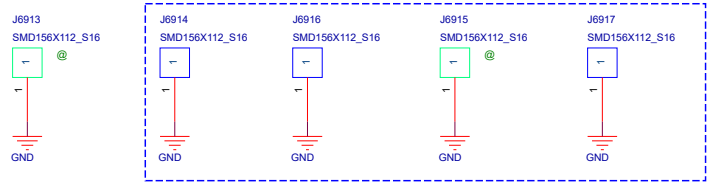
I/O board FUNC key
RD1_EE1



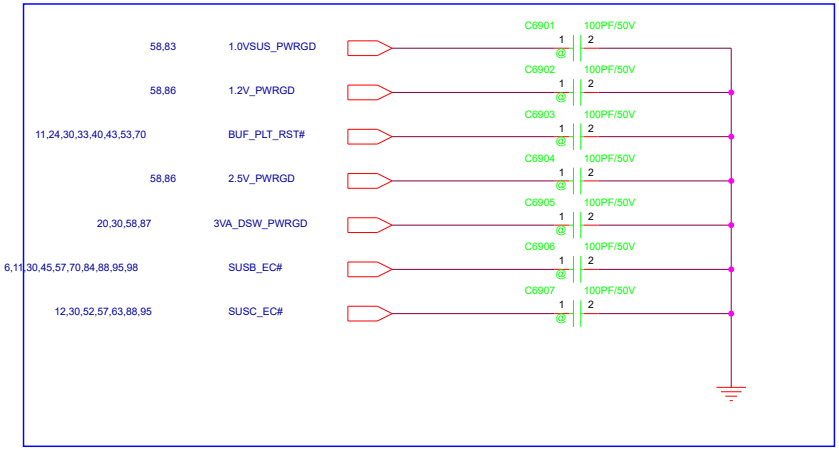


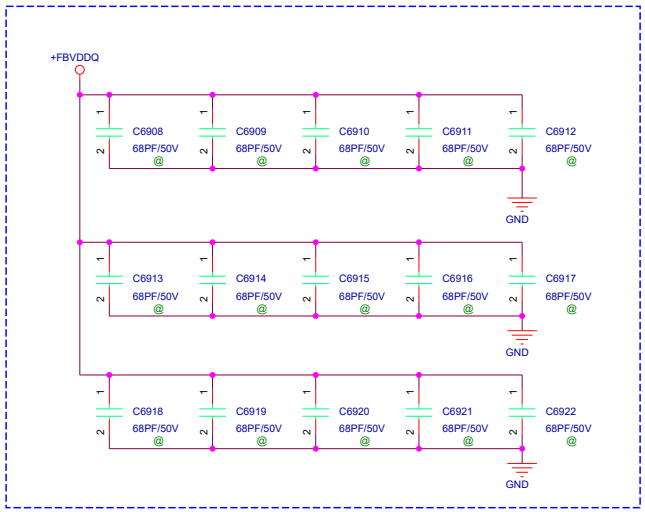


R1.2_17 EMI Reserve 100pf to Gnd



2015.10.07 For EMI Request





2016.06.20 For EMI Request

<Variant Name>

OTH_EMI

RD1_EE1

PCI EXPRESS_Graphics

REVERSED Type PCIE X16

GPU POWER GOOD Signal

NVVDD POWER GOOD LOOPBACK

Nvidia FAE Suggestion, add loopback circuit for protect NVVDD/MVVDS

GPU POWER SEQUENCE CONTROL

GPU_GPIO1

EC_GPIO

PCH_GPIO54

2016.06.21 Seq update

2016.06.20 GC6 Seq update

PCH_GPIO50, Pull down

GPU_GPIO4, +1V8_AON

+1V8_AON power rail

+3VS power rail

NVVDD EN

NVVDDS EN

PEXVDD EN

FBVDDQ EN

+1V8_AON EN

EMI

PLACE AT BALLS

Max:2800mA

PLACE OUTSIDE OF BGA

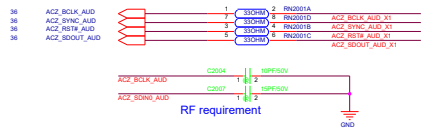
2016.07.18 Cost Reduce

Reverse PCIEG x 16

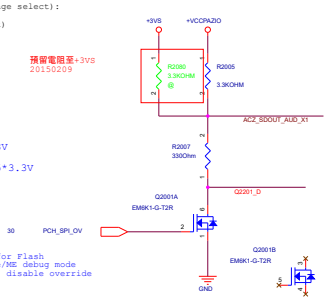
For EMI

ASUS	Project Name: G752VY			Rev: 2.0
Title : GPU_PCIE I/F				
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ashton_yang		
Date: Monday, July 25, 2016	Sheet: 70	of: 102		

HD Audio



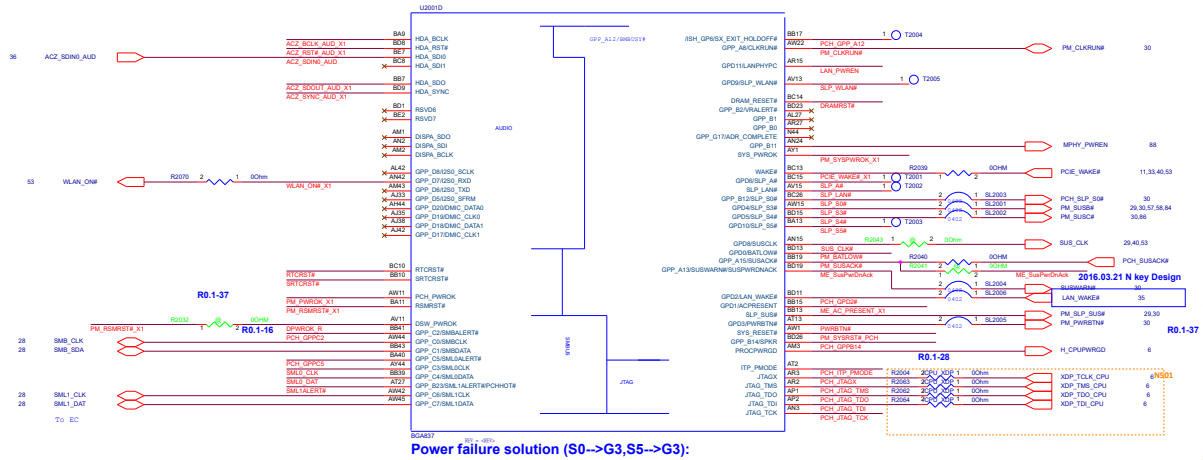
HDA_SYNC(On-Die PLL VR voltage select):
RlsIng edge of RSMRST# pin
High:1.5V, Low:1.8V (default)



預留電阻至+3VS
20150209

ACZ_SDOUT:
(1)PCH:
Internal PD 20k ohm,
VIL=0.35V,VIH=0.65~3.3V
(2)ALC269:
VIL<0.35*3.3V,VIH>0.65*3.3V

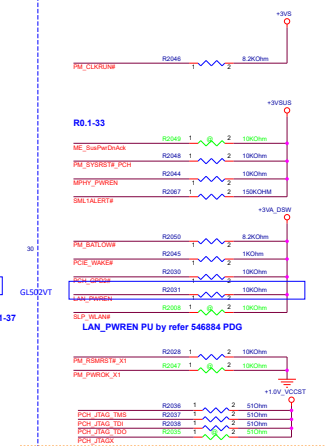
ACZ_SDOUT is a signal used for Flash
Descriptor security Override/ME debug mode
HIGH : get overrideen, LOW : disable override



Power failure solution (S0-->G3,S5-->G3):

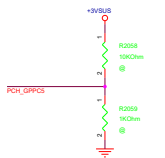
2016.03.21 N key Design

Main Board



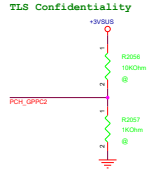
Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.0VSUS	+VCCST	+1.0V_VCCST	
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	+VCCPAZIO
		+3VS		

eSPI or LPC



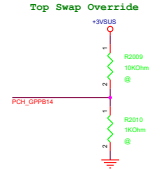
PCH_GPPC5: weak internal pull down	
PU	eSPI
PD	LPC (default)

TLS Confidentiality



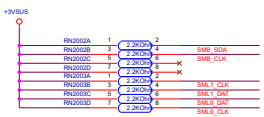
PCH_GPPC2: weak internal pull down	
PU	Enable
PD	Disable (default)

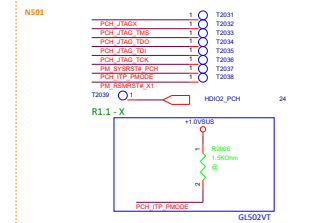
Top Swap Override

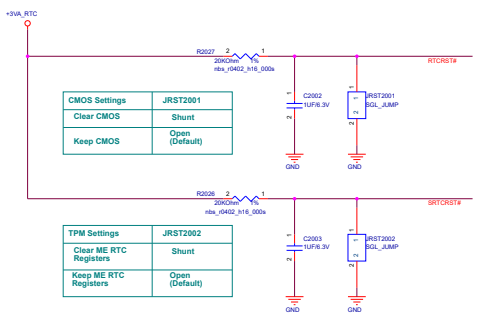


PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

SMBUS

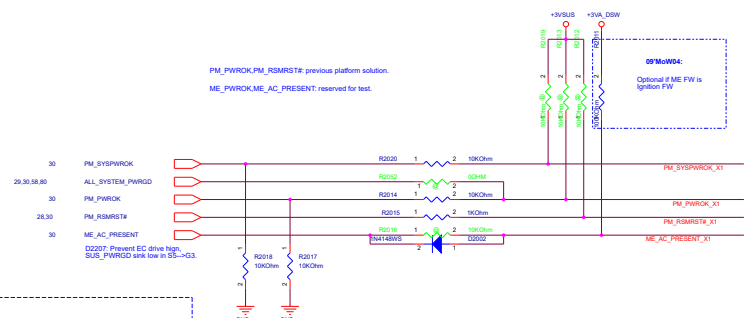






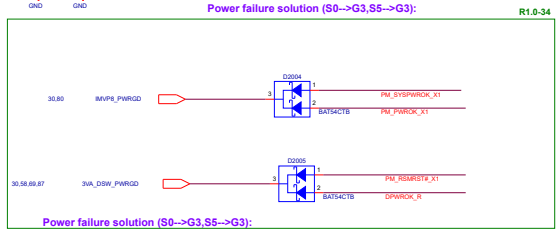
CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

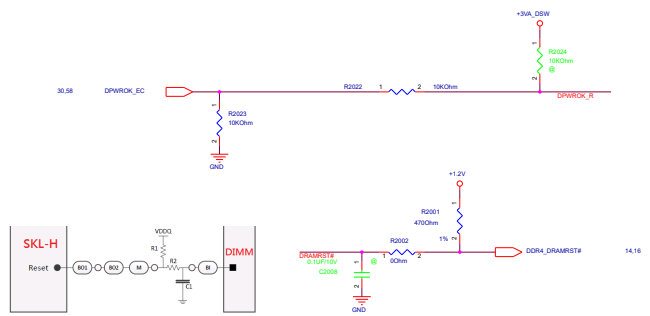
TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

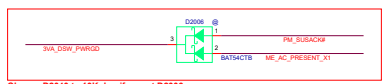


Power failure solution (S0-->G3,S5-->G3):

R1.0-34



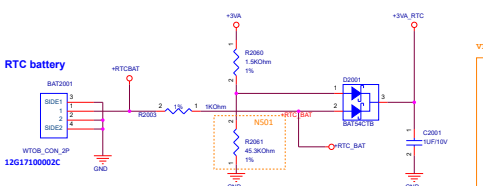




Change D2040 to 10Kohm if mount D2006

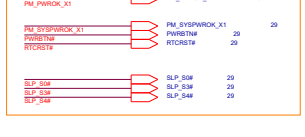
R1.1-03

Deep SX discharge (S0-->DSX,S5-->DSX)

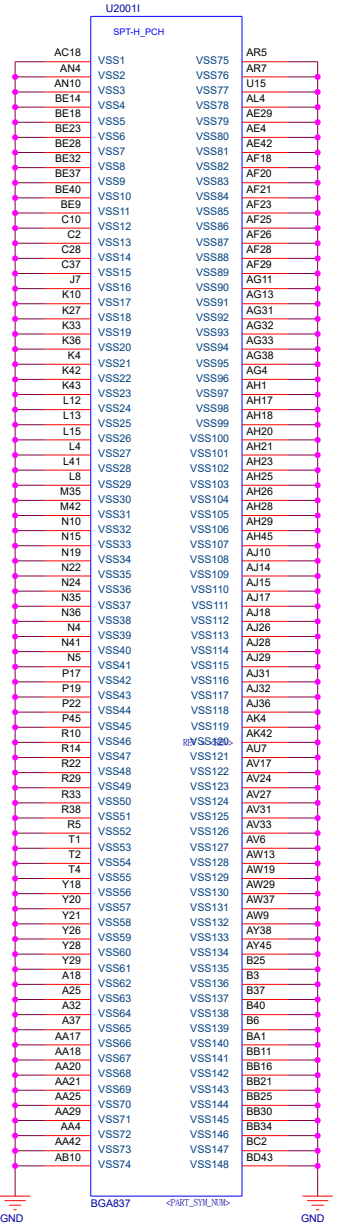


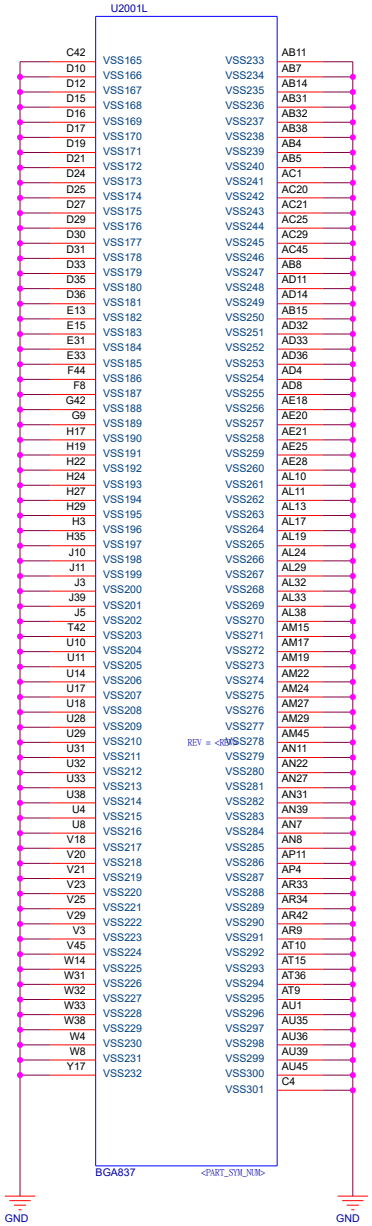
USE RTC Battery:
P/N: 0B100-00020300 BATT-LI CR2032 3V/220mAH
P/N: 0B100-00020400 BATT-LI CR2032 3V/220mAH

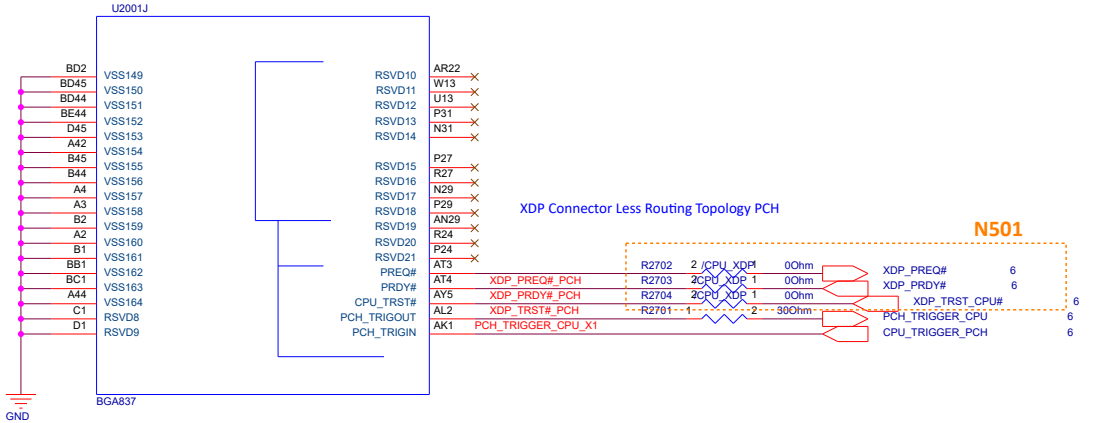
VL1.0-09



Project Name	GL502	Rev	1.0
Title :	PCH-CPT(1)SATA,HDA,RTC,JTAG		
Size	Custom	Dept.:	ASUSTeK COMPUTER
Engineer:	RD1_EE1		
Date:	Monday, July 25, 2016	Sheet	20 of 102







Project Name: GL502			Rev: 1.0
Title : PCH-CPT(8)_POWER,GND			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: RD1_EE1	
Date: Monday, July 25, 2016	Sheet 27 of 102		

Rev	Date	Description
R1.0	2015/10/30	01.Page 06 EDP Disable CFG4 Pull Down 02.Page08 VCCIO Add C0805/C0836 03.Page 70 Reserve optimus R7019 04.Page 14 +2.5V Add C1429/C1430 05.Page 26 Add C2651/C2644/C2645/C2648/C2649/C2650 Redule Power Noise 06.Page 26 Add C2640/C2641/C2652/C2643/C2657/C2658/C2659 Redule Power Noise 07.Page 26 Change R2601/R2602/R2607/R2623 From Resistor to Short Lane 08.Page 48 Reserve Level Shift for AUX Signal 09. Page56.Reserve Samsung LED Issue 10.Page 32 Change PS_ON Control EC_Rst# 11.Page 43 Add EMI Solution /Page 36 C3627,R3623 12.Page 438 Add EMI Solution R4832 for USB Noise 13.Page 48 1.5V HDMI LDO Change 14.Page 71/77C77103/C77104/C77109/C7101/C7102/C7167 Package change 0603
R1.1	2015/11/25	01.Page 47. Follow Design IP 02.Page 79. NV Suggest ADD IFPCD Power
R1.2	2015/12/11	01.Page 46. Modify CLK5_PCIE_USB31/CLK5_PCIE_USB31# 02.Page 34. 2nd Source Suggest(follow GL502VT) 03.Page 32. auto boot after press Power button 4 sec to shutdown 04.Page 25 Add R2543/R2544 Fix LED Power on Issue 05.Page 25 modify shortland for decrease voltage drop 06.Page 52/63 Remove Test Point T5201/T6301 07.Page 78 Remove C7804/C7906/C7809,Pleacment consider 08.Page 26 Add C2658/C2652/C2654/C0840 fix power noise 09.Page 78 Add C7804/C7809 fix +PEX_VDD power noise 10.Page 88 Remove JP/MOS Add Power shape 11.Page 77 Add C77194~C77201 fix F8VDDQ Noise 12.Page 88 Remove R +1.0VM_VCCMPHY 13.Page 69 Remove J6915 .Change EMI Gasket (13040-00440000) 14.Page 48 Add EMI Solution RN4804/RN4805/RN4896/RN4807 15.Page 22 TXC Crystal Report Suggest Modify C2201/C2201 C3306/C3307 C4305/C4320 16.Page 67 Follow ME DXF Modify H6732/H6745/H6746/H6747 17.Page 69 EMI Reserve C6901~C6907 100pf fix EMI Issue 18.Page 49 Remove GPU Breaket H6724~H6727 19.Page 43 Remove R4306/R4308 for Sequence request 20.Page 70 Remove R7018 Add R7028 fix NV Sequence issue 21.Page 71 Modify 1uf Change 0.1uf fix +NVDD Power Noise

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

Revision History

RD1_EE1

ASUSTeK COMPUTER

D GL502 1.0

Monday, July 25, 2016 102 102

UX303JA Power-On Sequence Timing Diagram Rev.0.1

AC-IN Mode

1 +3VA/+5VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 VSUS_ON

+3VSUS/+5VSUS

(PCH to EC) 4 ME_SusPwrDnAck

(power to EC) 5 SUS_PWRGD

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 AC_PRESENT

(to EC) 8 PWR_SW#

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 PM_SLP_A#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/SLP_LAN#

(PCH to EC) (PCH to power) +1.1VM_LAN

(EC to power) ME_SLP_M_EC#

+1.1VM/+3VM

(EC to power) 13 SUSC_EC#

+0.6V/+1.2V/+1.8V/+3V/+5V

(EC to power) 14 SUSB_EC#

+1.05VS/+1.2VS//+1.8VS/+3VS/+5VS

(power to EC) ME_+VM_PWRGD

(EC to PCH) ME_PWROK

15 SYSTEM_PWRGD

+VTT_CPU

(CPU to power) GFX_VR_ON

16 +VTT_CPU_PWRGD/ 17 H_VTTPWRGD (power to CPU)

GFX_VID

+VGFX_CORE

(power to EC) GFX_PWRGD

18 ALL_SYSTEM_PWRGD

(EC to power) CPU_VRON

19 +VCCIN

CLK_PWRGD

(inversion of CLK_EN#)

(power to EC) 20 CORE_PWRGD

(EC to PCH) 21 PM_PWROK

(PCH to CPU) H_DRAM_PWRGD

(PCH to CPU) H_CPUPWRGD

(PCH to CPU) 22 BUF_PLT_RST#

(pull up to +3VSUS)

T0=20ms (spec.>=10ms)

T1<200ms(check)

(falling edge)

T2=50ms

T3=2ms (spec.>=1ms)

T4=1.25ms

T5=60us(typ.)

T6=110ms (spec.>=99ms)

T7=10~100us

T8=3~20ms

T9=10ms

<Variant Name>

Power On Timing

EE

ASUSTeK COMPUTER

C GL502 1.0

Monday, July 25, 2016 101 102

UX303JA Power-On Sequence Timing Diagram Rev.0.1

AC-IN Mode

1 +3VA/+5VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 VSUS_ON

+3VSUS/+5VSUS

(PCH to EC) 4 ME_SusPwrDnAck

(power to EC) 5 SUS_PWRGD

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 AC_PRESENT

(to EC) 8 PWR_SW#

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 PM_SLP_A#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/SLP_LAN#

(PCH to EC) (PCH to power)

+1.1VM_LAN

(EC to power) ME_SLP_M_EC#

+1.1VM/+3VM

(EC to power) 13 SUSC_EC#

+0.6V/+1.2V/+1.8V/+3V/+5V

(EC to power) 14 SUSB_EC#

+1.05VS/+1.2VS//+1.8VS/+3VS/+5VS

(power to EC) ME_+VM_PWRGD

(EC to PCH) ME_PWROK

15 SYSTEM_PWRGD

+VTT_CPU

(CPU to power) GFX_VR_ON

16 +VTT_CPU_PWRGD/ 17 H_VTTPWRGD

(power to CPU)

GFX_VID

+VGFX_CORE

(power to EC) GFX_PWRGD

18 ALL_SYSTEM_PWRGD

(EC to power) CPU_VRON

19 +VCCIN

CLK_PWRGD

(inversion of CLK_EN#)

(power to EC) 20 CORE_PWRGD

(EC to PCH) 21 PM_PWROK

(PCH to CPU) H_DRAM_PWRGD

(PCH to CPU) H_CPUPWRGD

(PCH to CPU) 22 BUF_PLT_RST#

(pull up to +3VSUS)

T0=20ms (spec.>=10ms)

T1<200ms(check)

(falling edge)

T2=50ms

T3=2ms (spec.>=1ms)

T4=1.25ms

T5=60us(typ.)

T6=110ms (spec.>=99ms)

T7=10~100us

T8=3~20ms

T9=10ms

<Variant Name>

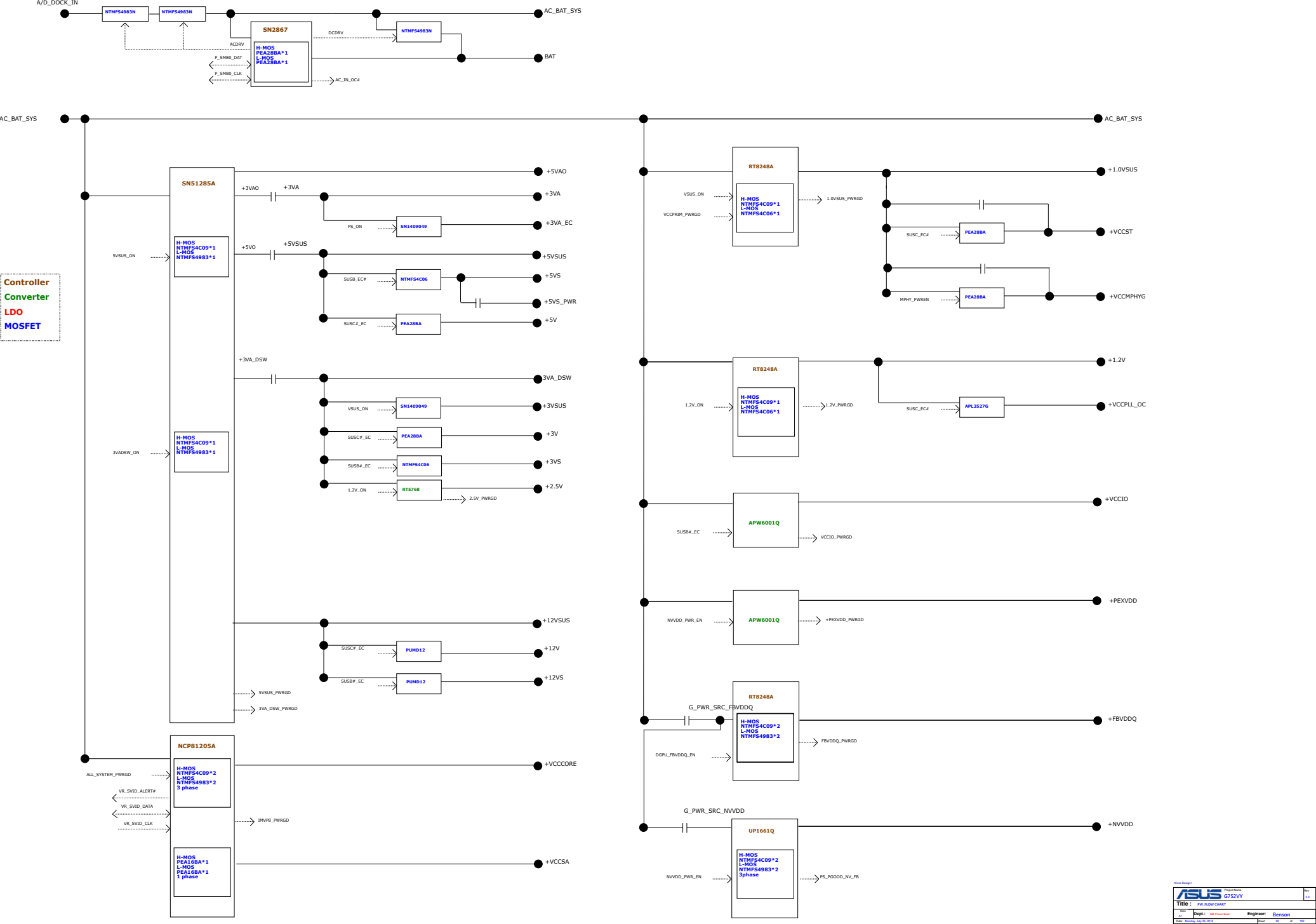
Power On Timing

EE

ASUSTeK COMPUTER

C GL502

Monday, July 25, 2016 100 102 1.0


A/D_DOCK_IN
NTMFS4983N
NTMFS4983N
AC_BAT_SYS
SN2867
DCDRV
NTMFS4983N
ACDRV
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
BAT
P_SMB0_DAT
P_SMB0_CLK
AC_IN_OC#
AC_BAT_SYS
AC_BAT_SYS
Controller
Converter
LDO
MOSFET
SN51285A
+5VAO
+3VAO
+3VA
+3VA
PS_ON
SN1409049
+3VA_EC
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4983*1
5VSUS_ON
+5VO
+5VSUS
+5VSUS
SUSB_EC#
NTMFS4C06
+5VS
+5VS_PWR
SUSC#_EC
PEA28BA
+5V
+3VA_DSW
3VA_DSW
VSUS_ON
SN1409049
+3VSUS
SUSC#_EC
PEA28BA
+3V
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4983*1
3VADSW_ON
SUSB#_EC
NTMFS4C06
+3VS
1.2V_ON
RT5768
+2.5V
2.5V_PWRGD
+12VSUS
SUSC#_EC
PUMD12
+12V
SUSB#_EC
PUMD12
+12VS
5VSUS_PWRGD
3VA_DSW_PWRGD
NCP81205A
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4983*2
3 phase
ALL_SYSTEM_PWRGD
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
+VCCCORE
IMVP8_PWRGD
H-MOS
PEA168A*1
L-MOS
PEA168A*1
1 phase
+VCCSA
AC_BAT_SYS
RT8248A
VSUS_ON
VCCPRIM_PWRGD
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C06*1
1.0VSUS_PWRGD
+1.0VSUS
SUSC_EC#
PEA28BA
+VCCST
MPHY_PWREN
PEA28BA
+VCCMPHYG
RT8248A
1.2V_ON
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C06*1
1.2V_PWRGD
+1.2V
SUSC_EC#
APL3527G
+VCCPLL_OC
APW6001Q
SUSB#_EC
VCCIO_PWRGD
+VCCIO
APW6001Q
NVVDD_PWR_EN
+PEXVDD_PWRGD
+PEXVDD
RT8248A
G_PWR_SRC_FBVDDQ
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4983*2
FBVDDQ_PWRGD
+FBVDDQ
DGPU_FBVDDQ_EN
G_PWR_SRC_NVVDD
UP1661Q
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4983*2
3phase
+NVVDD
NVVDD_PWR_EN
PS_PGOOD_NV_FB
<Core Design>
ASUS
Project Name
G752VY
Rev
2.0
Title :
PW_FLOW CHART
Size
A4
Dept.:
NB Power team
Engineer:
Benson
Date: Monday, July 29, 2019
Sheet
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of
100

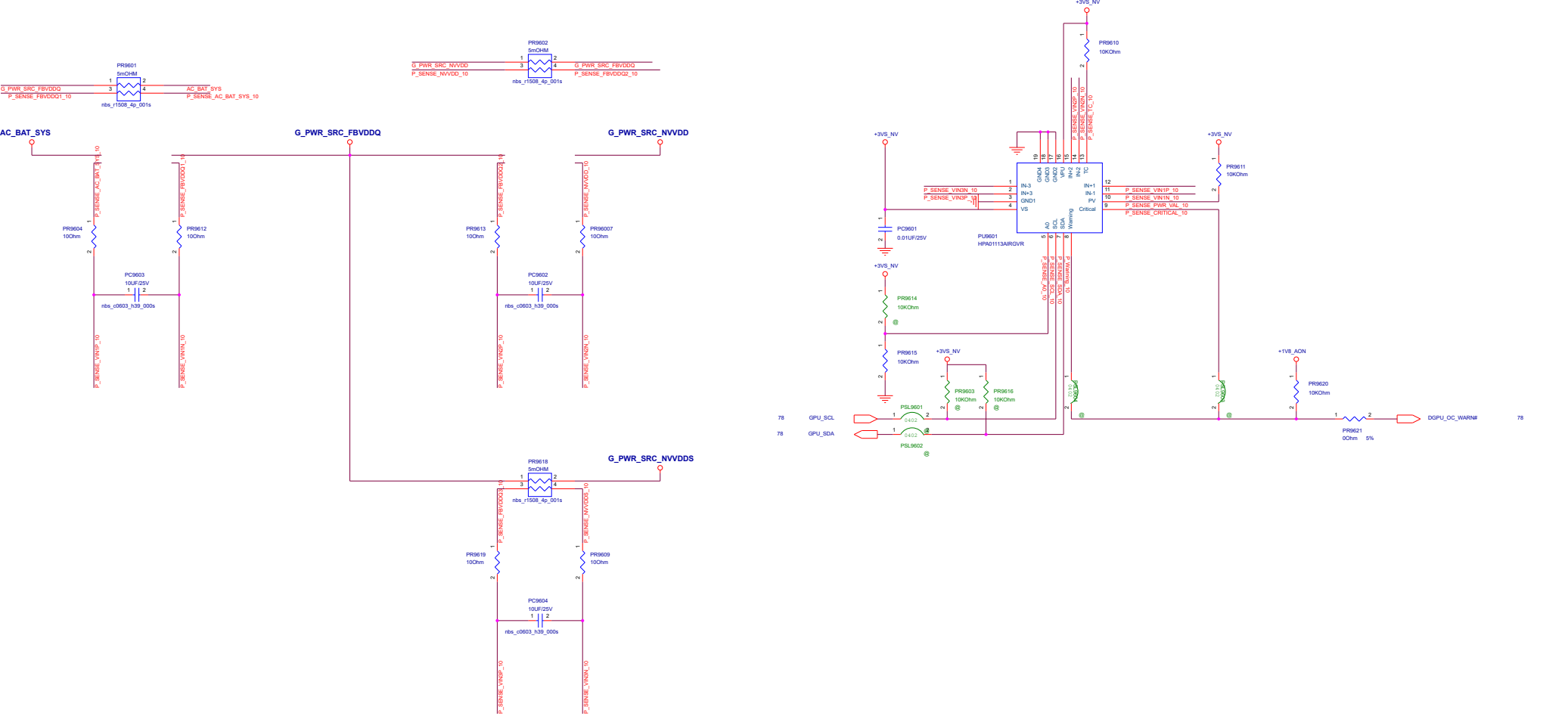
<Variant Name>

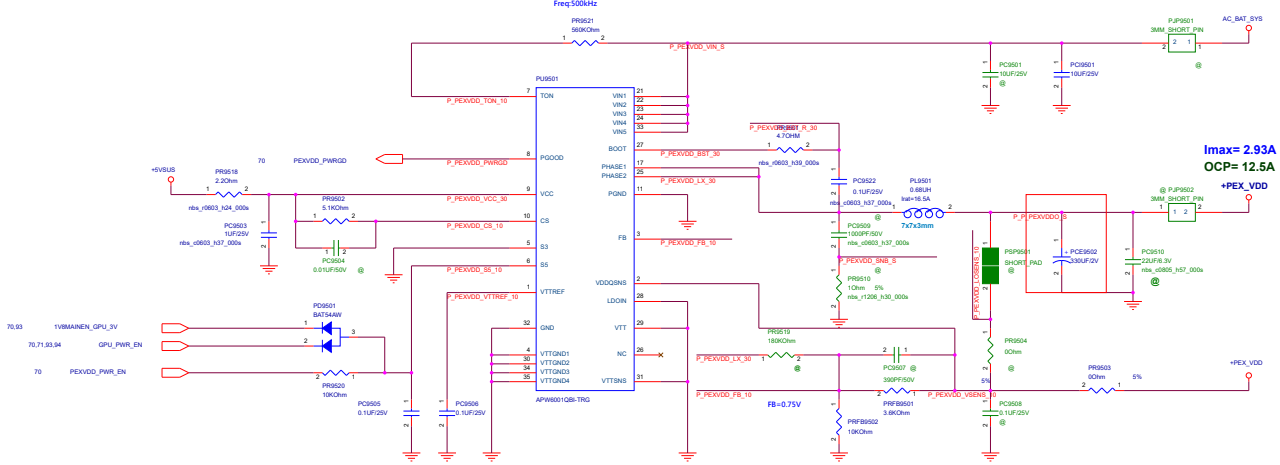
	Project Name **GL502VM**	Rev 2.0

Title : PW_OV

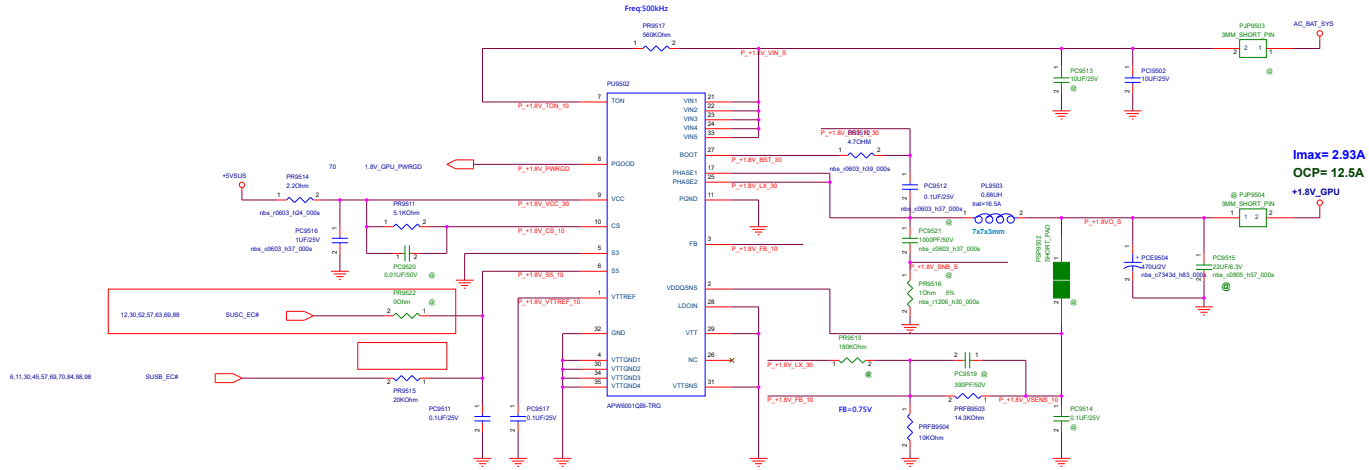
Size		
A	**Dept.:** NB Power team	**Engineer:** Edison

Date: Monday, July 25, 2016	Sheet 97	of	102


PR9601
5mOHM
G_PWR_SRC_FBVDDQ
P_SENSE_FBVDDQ1_10
AC_BAT_SYS
P_SENSE_AC_BAT_SYS_10
nbs_r1508_4p_001s
PR9602
5mOHM
G_PWR_SRC_NVVDD
P_SENSE_NVVDD_10
G_PWR_SRC_FBVDDQ
P_SENSE_FBVDDQ2_10
nbs_r1508_4p_001s
AC_BAT_SYS
G_PWR_SRC_FBVDDQ
G_PWR_SRC_NVVDD
G_PWR_SRC_NVVDDS
PR9604
10Ohm
PR9612
10Ohm
PC9603
10UF/25V
nbs_c0603_h39_000s
PR9613
10Ohm
PR9607
10Ohm
PC9602
10UF/25V
nbs_c0603_h39_000s
PR9618
5mOHM
nbs_r1508_4p_001s
PR9619
10Ohm
PR9609
10Ohm
PC9604
10UF/25V
nbs_c0603_h39_000s
+3VS_NV
PR9610
10KOhm
PR9611
10KOhm
PC9601
0.01UF/25V
PU9601
HPA01113AIRGVR
IN-3
IN+3
GND1
VS
IN+1
IN-1
PV
Critical
A0
SCL
SDA
Warning
PR9614
10KOhm
PR9615
10KOhm
PR9603
10KOhm
PR9616
10KOhm
PSL9601
PSL9602
+1V8_AON
PR9620
10KOhm
PR9621
0Ohm 5%
GPU_SCL
GPU_SDA
DGPU_OC_WARN#
78



PRFB9501	APW6001_Vout
3.6kohm	1.0V
4.02kohm	1.05V
14.2kohm	1.8V

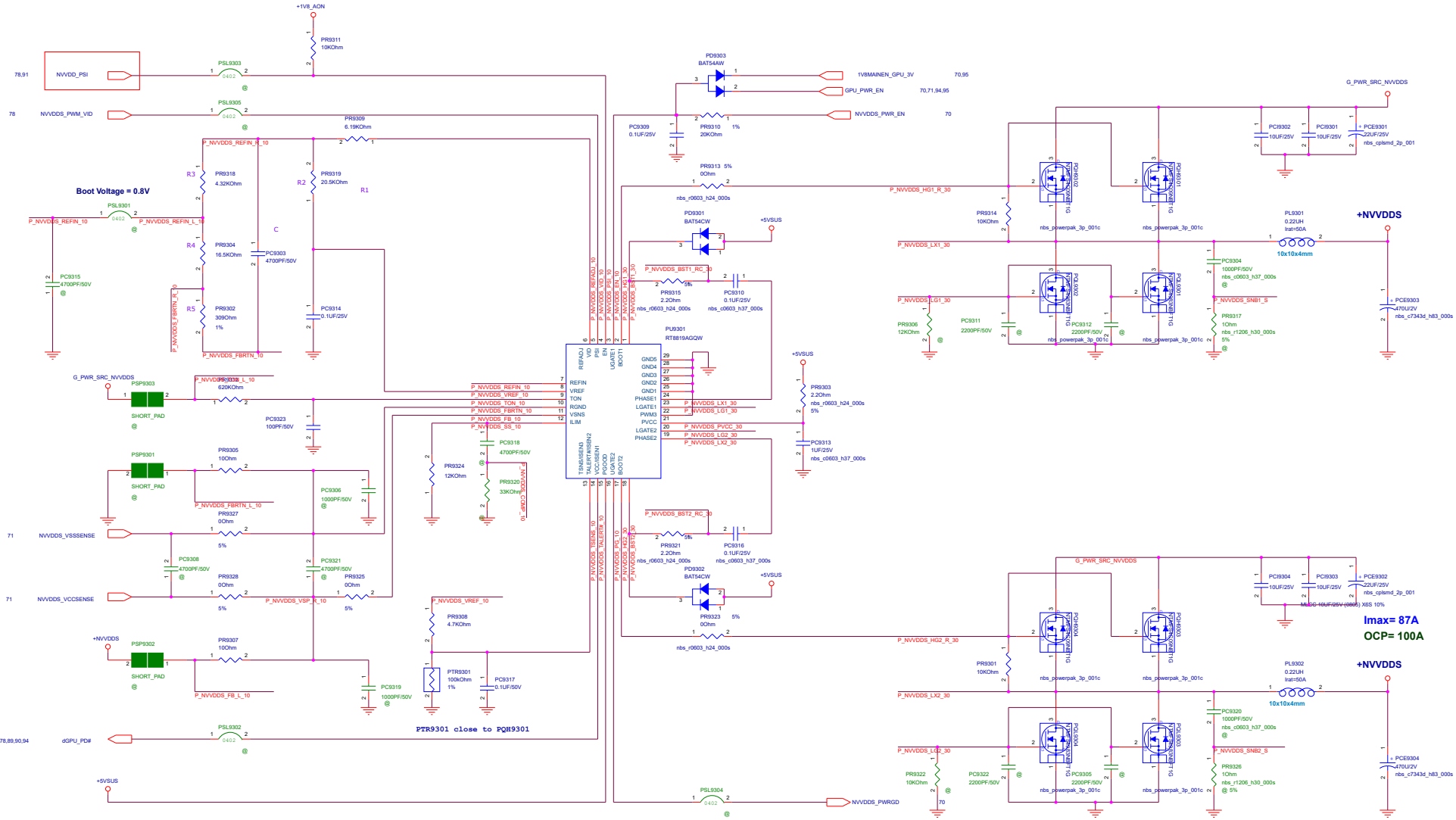


PRFB9503	APW6001_Vout
3.6kohm	1.0V
4.02kohm	1.05V
14.3kohm	1.8V

<Variant Name>

ASUS	Project Name: GL502VM	Rev: R1.0
Title :	PW_PEX_VDD/+1.8V_GPU	
Size: A2	Dept.: NB Power Team	Engineer: Edison
Date: Monday, July 25, 2016	Sheet 95 of 102	

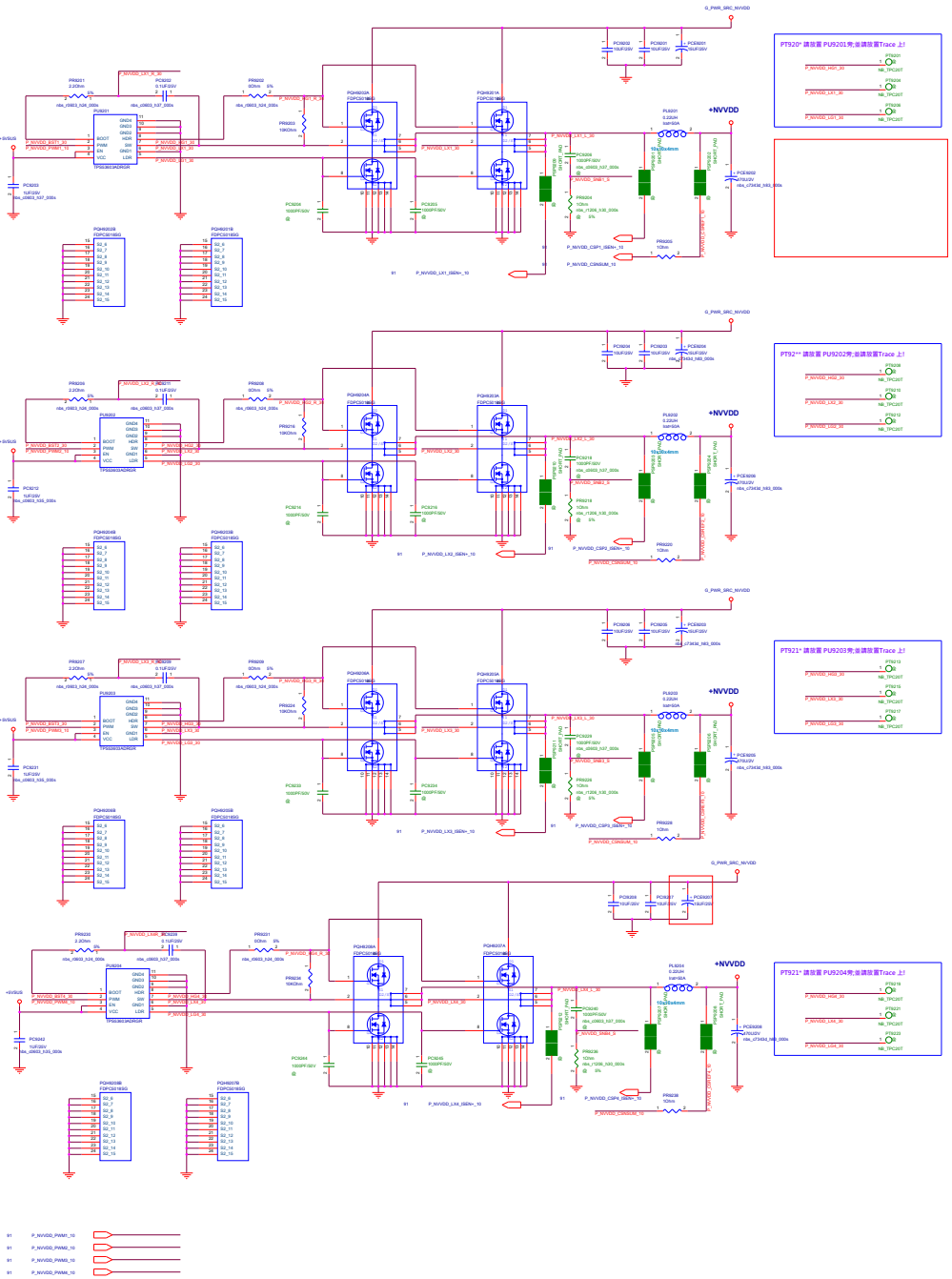
+NVVDDS [For DGPU]



<Variant Name>

ASUS	Project Name: GL502VM	Rev: R1.0
Title : PW_+NVVDDS		
Size: C	Dept.: NB Power Team	Engineer: Edison
Date: Monday, July 25, 2016	Sheet 93 of 102	

+NVVDD [For DGPU]



<Variant Name>

ASUS Project Name: GL502VM Rev: 31.0

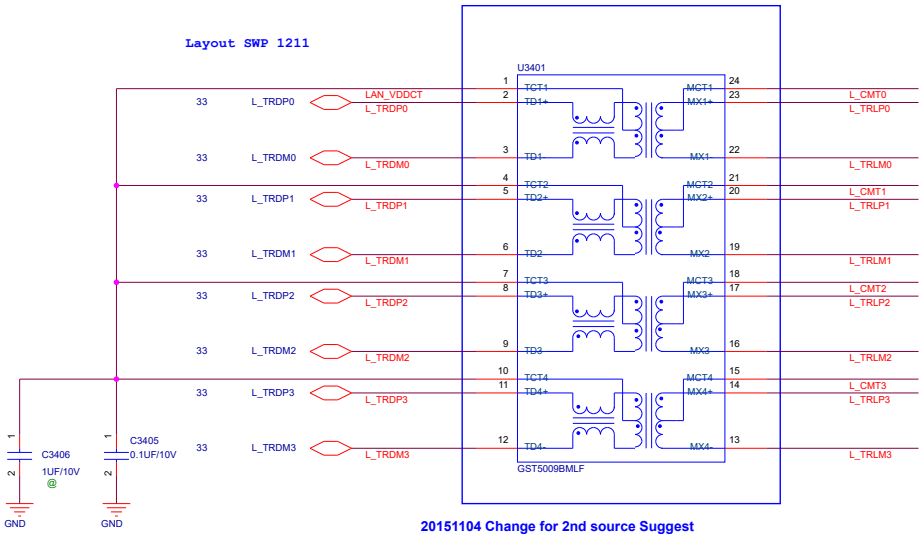
Title : PW_+NVVDD (2)

Size: A1 Dept.: NB Power Item Engineer: Edison

Date: Monday, July 23, 2018 Sheet 92 of 102

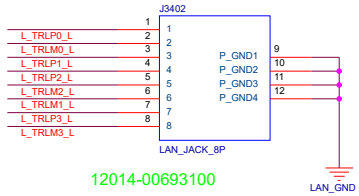
R1.2_02 follow GL502VT

Layout SWP 1211



20151104 Change for 2nd source Suggest

LAN Connector

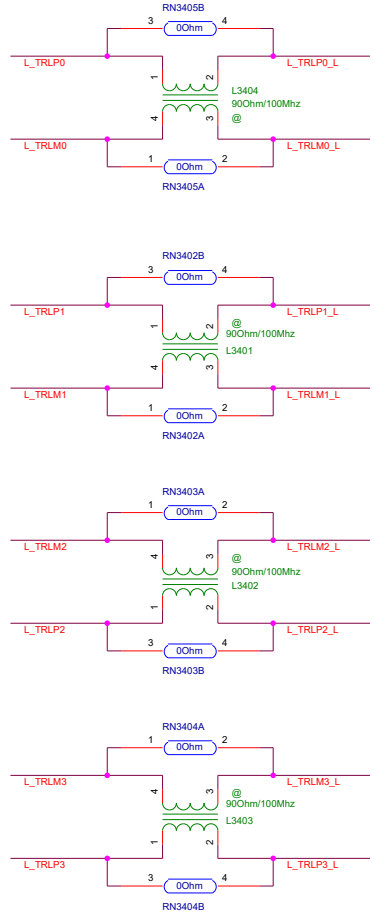


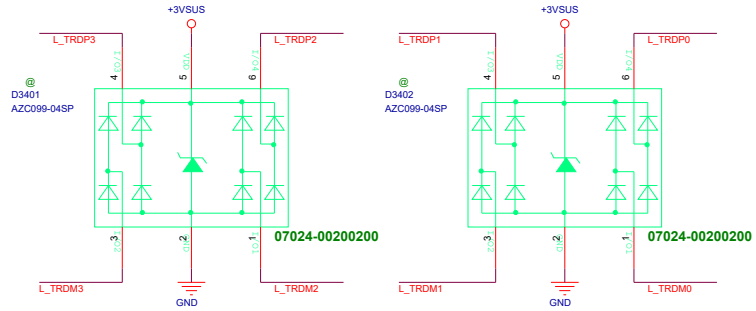
12014-00693100

J3402 LAN Jack

1st Source: P/N:12014-00161700 FOXCONN/JM3611-NS640003-7H

2nd Source: P/N:12014-00035500 SINGATRON/2RJ1648-000111F

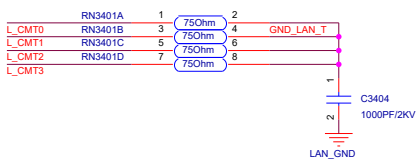




D3401,D3402 ESD Diode

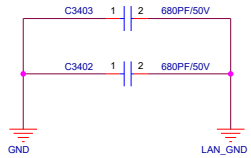
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



GND_LAN_T 上禁止加任何零件

2012/2/16 EMI



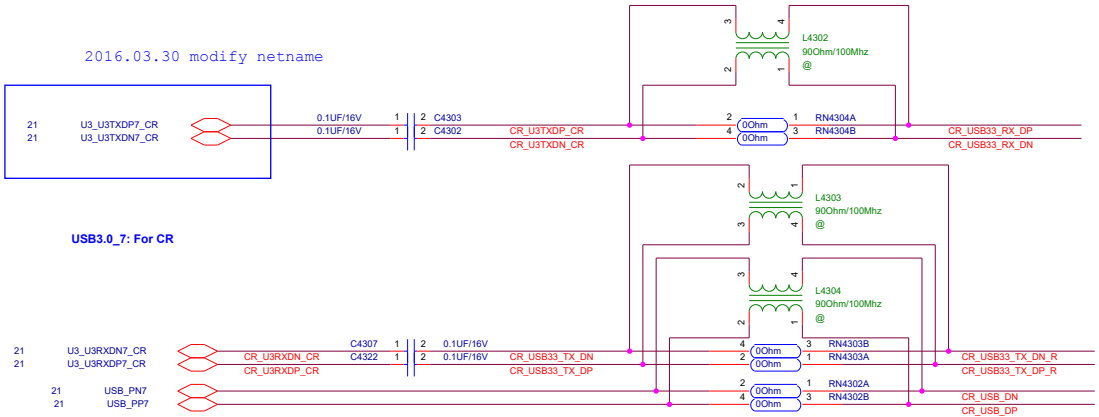
Place near chassis GND

ASUS	Project Name: GL502	Rev: 1.0
Title : LAN RJ45 Conn.		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD1_EE1
Date: Monday, July 25, 2016	Sheet 34 of 102	

CR I/O Conn. (MB)

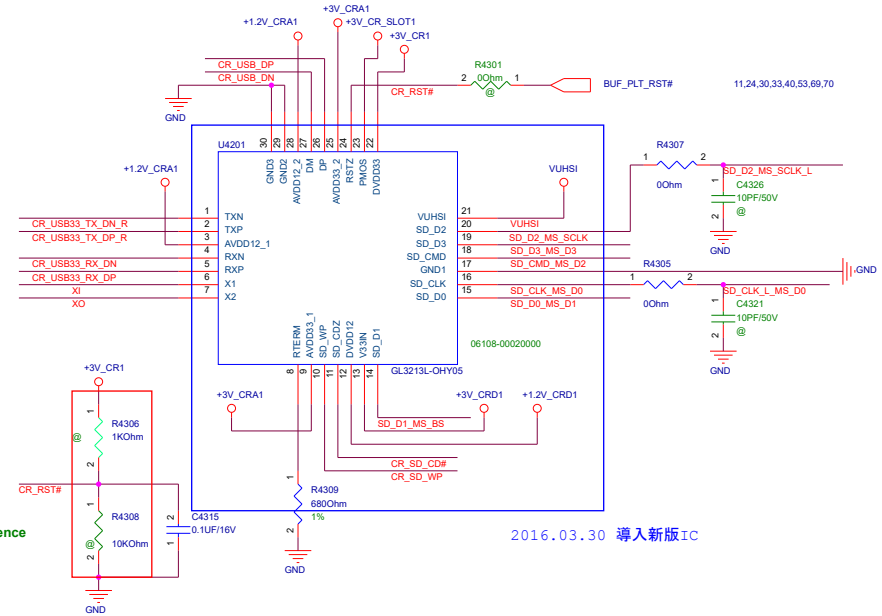
Main Board

2016.03.30 modify netname



USB3.0_7: For CR

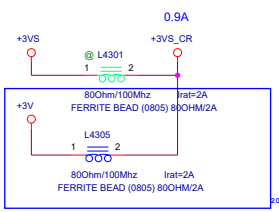
USB2.0_7: For CR



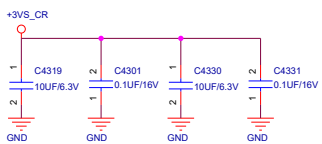
R1.2-18 Sequence

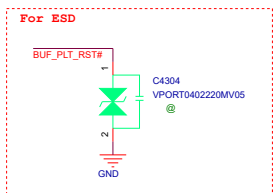
2016.03.30 導入新版IC

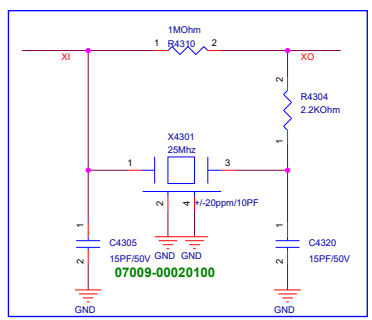
CardReader PWR



2016.03.18 slove the s3 redetect issue







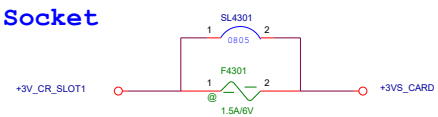
2016.07.22 Epson suggest

X4201: 25MHZ +/-20ppm/10pF (3225)

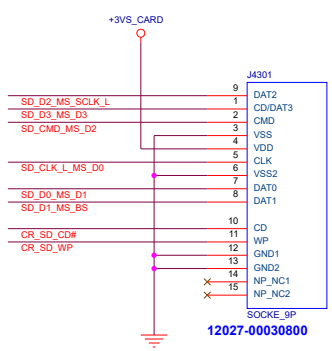
1st: P/N:07009-00020100 EPSON/FA-238G

2nd: P/N:07009-00020800 TXC/7V25000000

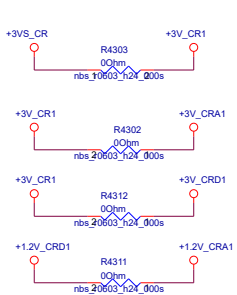
CR Socket

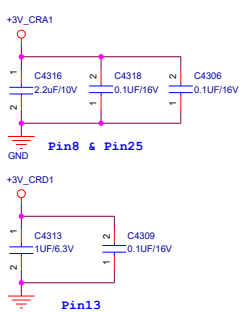


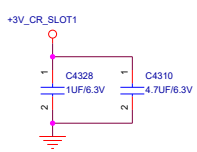
Reserved fuse for safety



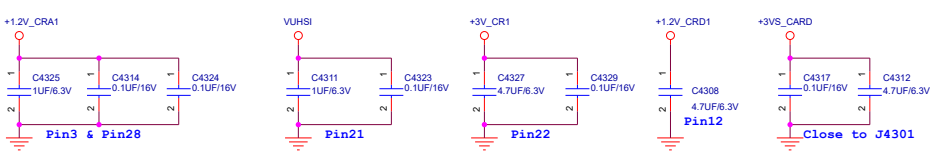
12027-00030800

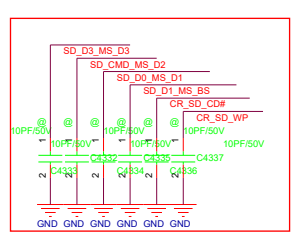






C4214, C4215 close to Pin23

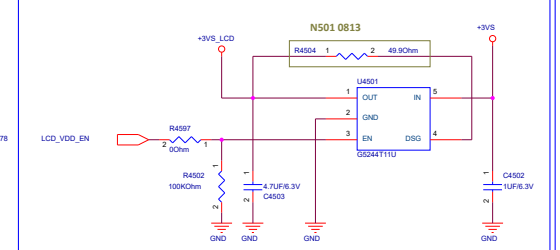




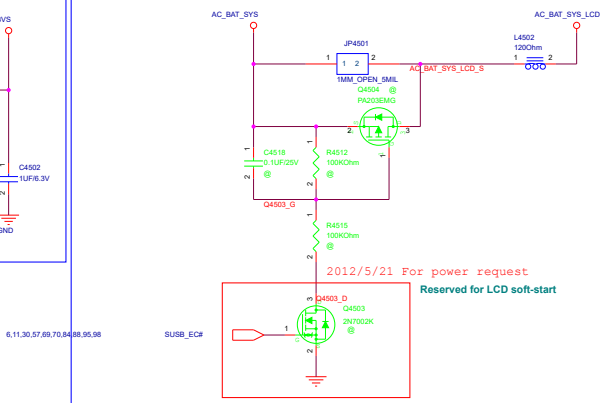
R1.0_011 Add EMI Solution

ASUS	Project Name: GL502		Rev: 1.0
Title : CB IO CON			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD1_EE1	
Date: Monday, July 25, 2016		Sheet 43 of 102	

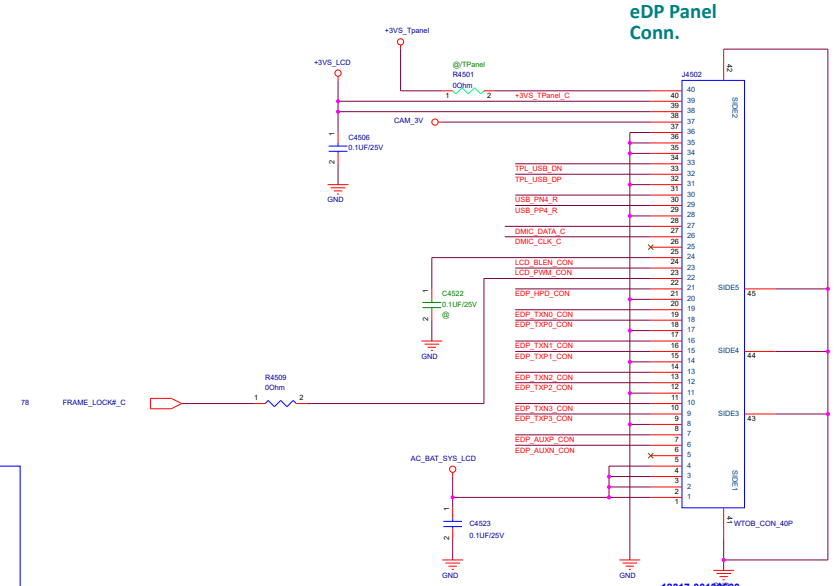
LCD Power switch



Panel BL Power



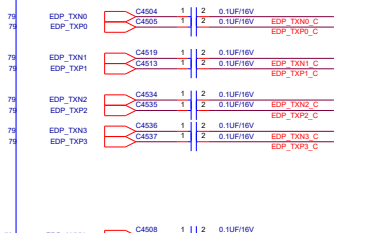
eDP Panel Conn.



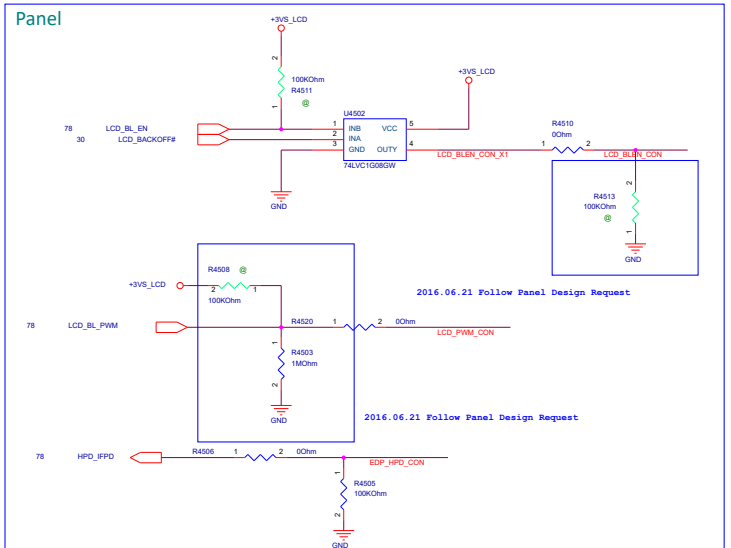
12017-00180000

S:12017-00180900

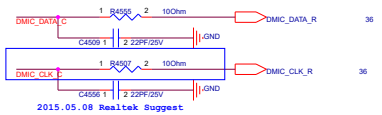
eDP from CPU



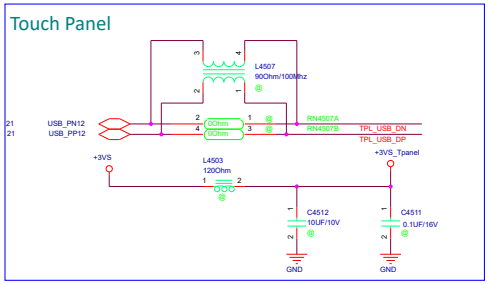
Panel



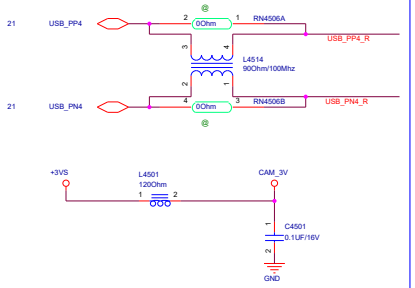
MIC



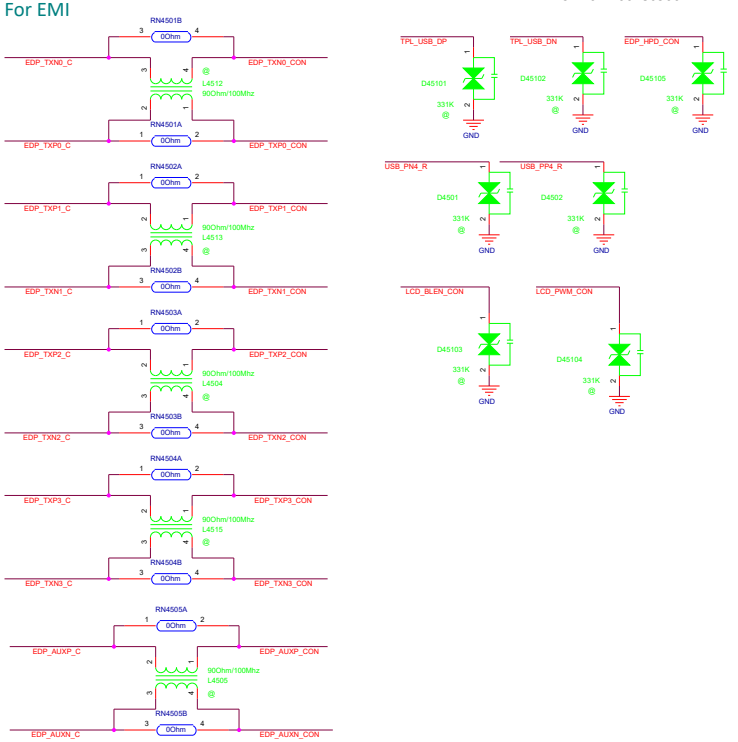
Touch Panel



Camera module



For EMI



<Variant Name>

CRT_eDP

RD1_EE1

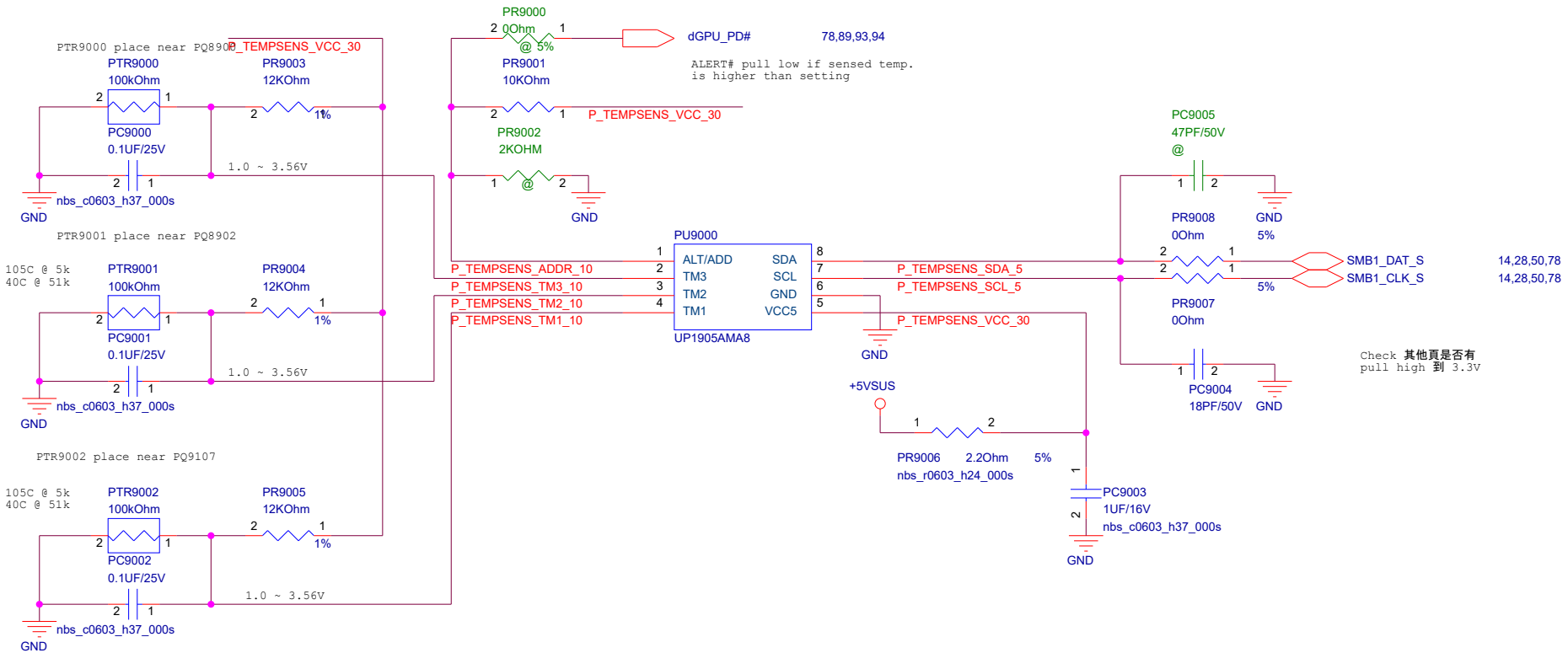
Main Board

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

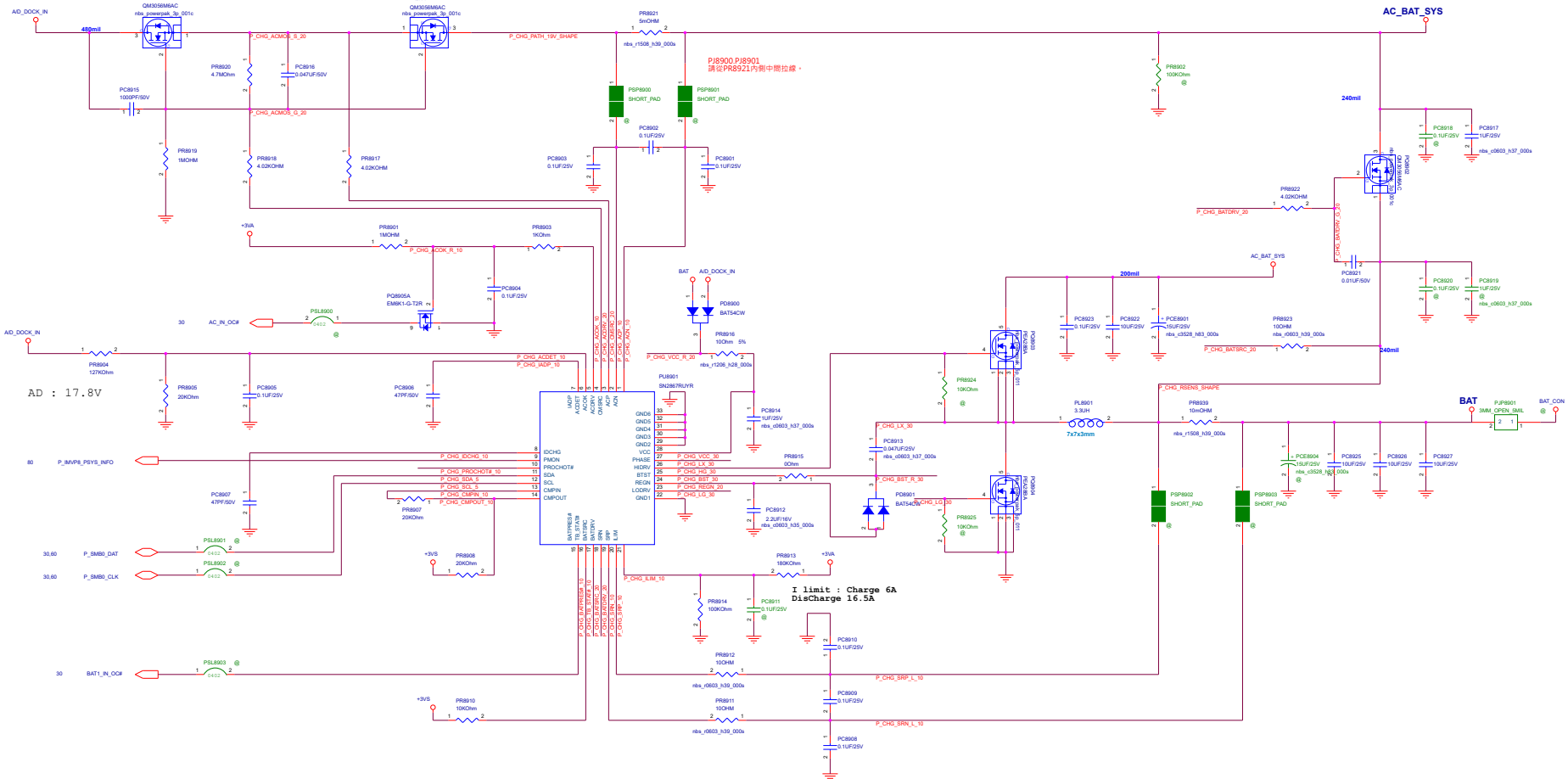
Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



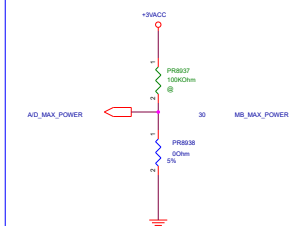
Project Name: GL502VM		Rev: 2.0
Title : PW_PROTECTION		
Size: A4	Dept.: NB Power team	Engineer: Edison
Date: Monday, July 25, 2016	Sheet 90 of 102	

Main Board

PR8921	<=40W	<=120W	>=120W
	20m	10m	5m
	10125-00048000	10G21DR01015111	10G21DR00515111

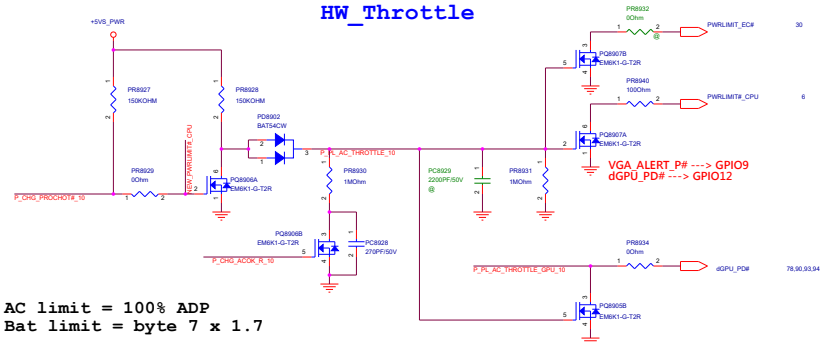


Adaptor select
total power = 90% ADP



Adaptor select		N Series	G Series
PR8921		10m	5m
PR8936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	300W
270K	2.4V	90W	330W
560K	2.8V	120W	400W

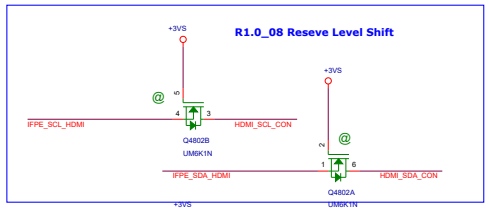
HW_Throttle

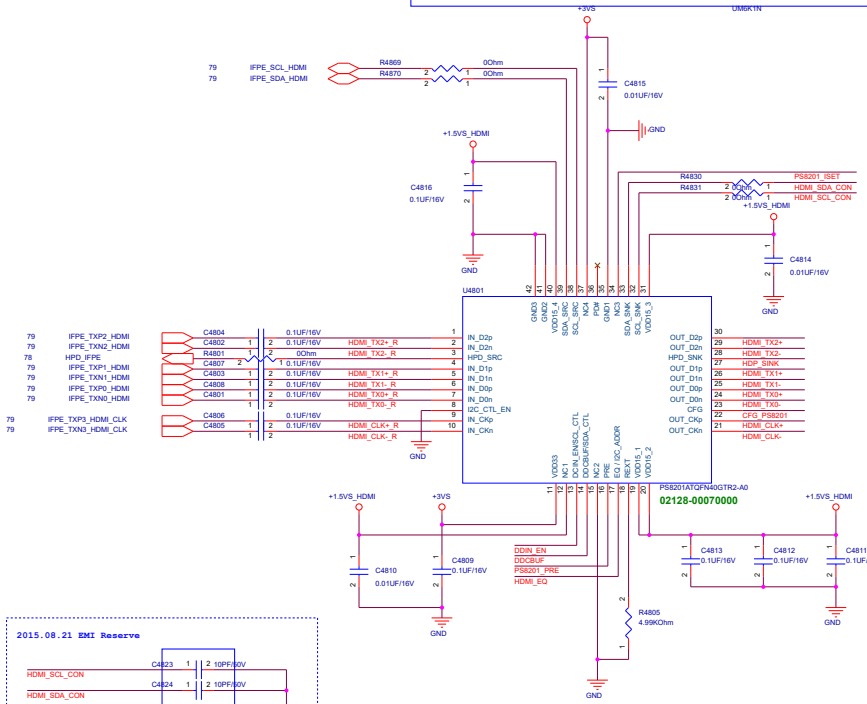


AC limit = 100% ADP
Bat limit = byte 7 x 1.7

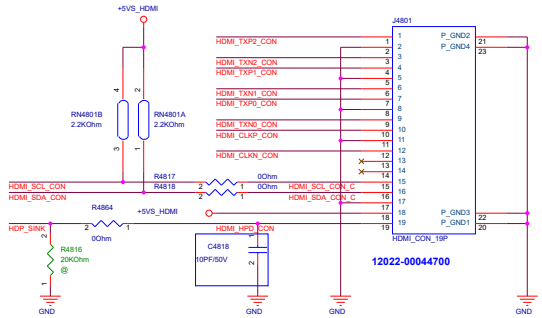
ASUS	Project Name: GL502VM		Rev: 2.0
Title : PW_CHARGER			
Size: A2	Dept.: NB Power team	Engineer: Edison	
Date: Monday, July 25, 2016	Sheet 89 of 102		

HDMI Active-Level Shift





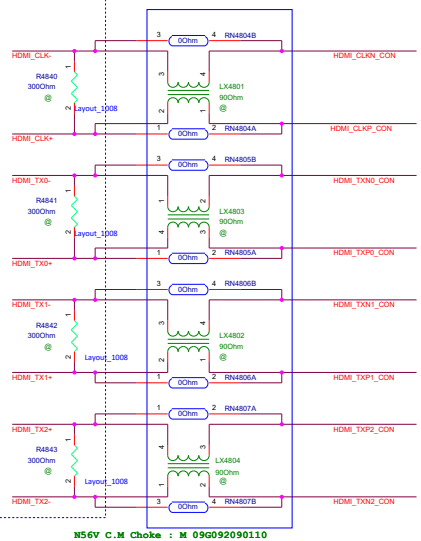
HDMI Conn.



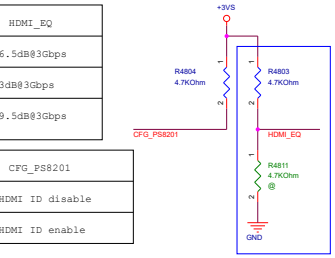
HDMI EMI

2016.05.11 EMI Reserve

2016.07.20 VR solution

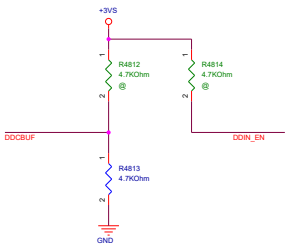


N56V C.M Choke : M 09G092090110



2016.07.20 VR solution

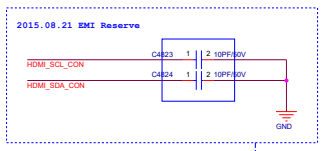
2016.07.20 VR solution



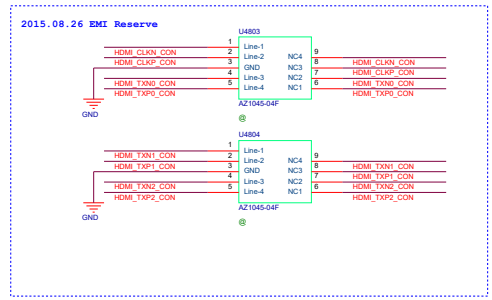
FIX can't read 4K2K HDMI Monitor EDID BUG

Reverse R4812, Mount R4813 Pull-down

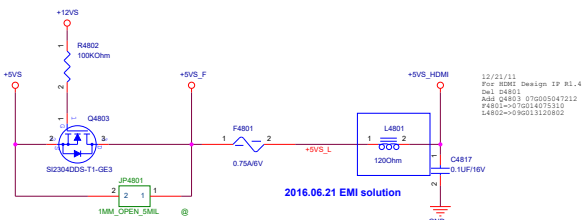
2015.08.21 EMI Reserve



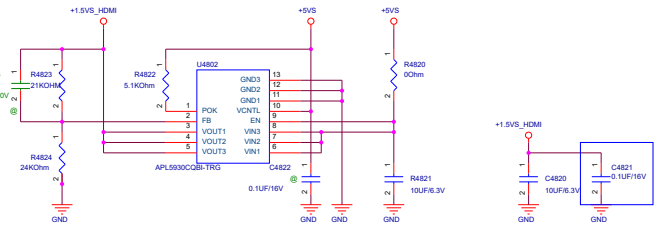
2015.08.26 EMI Reserve



HDMI PWR_+5VS_HDMI



HDMI LDO 1.5VS



Project Name	Rev
GL502	1.0

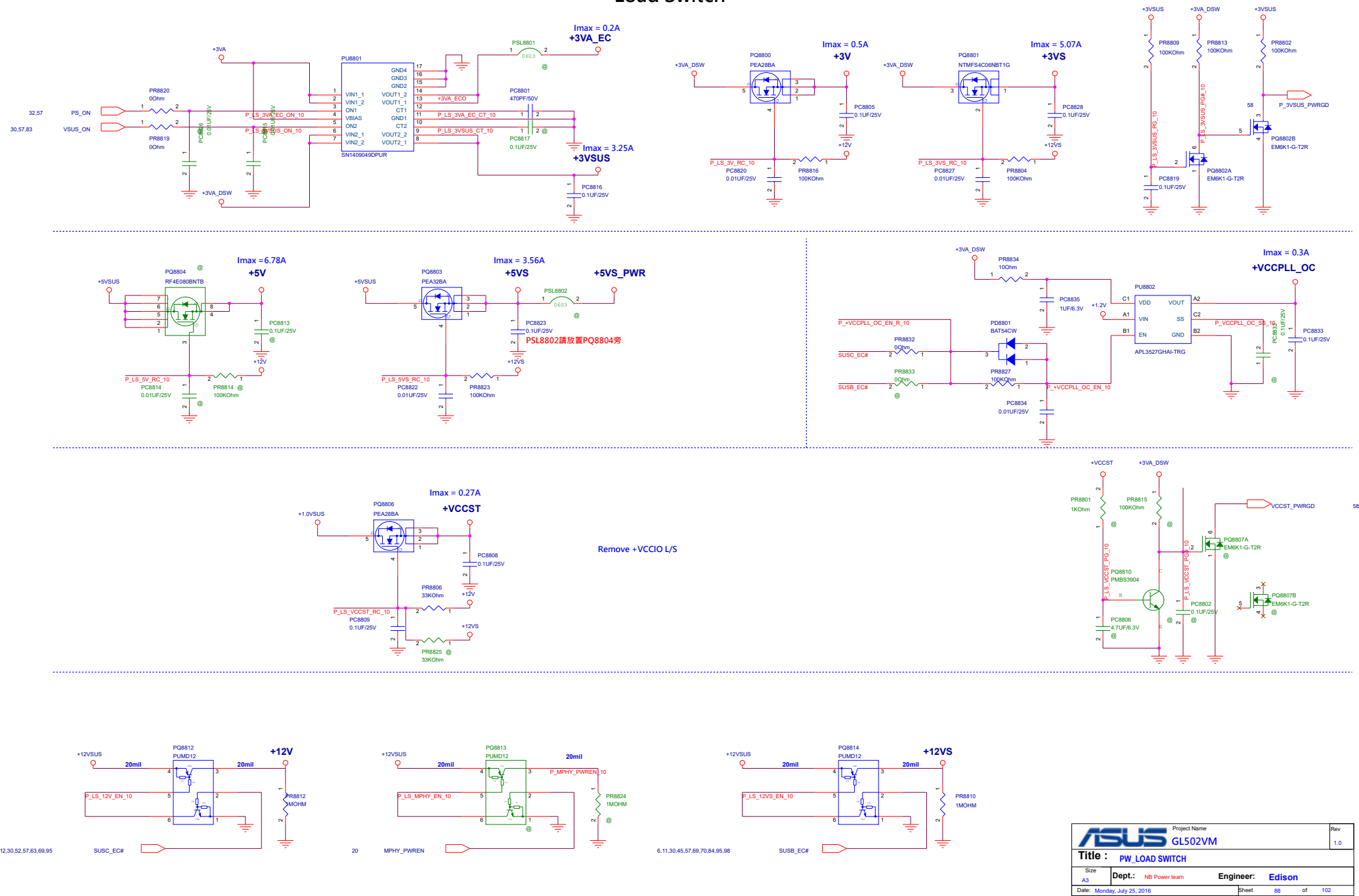
Title : HDMI Conn.

Size	Dept.	Engineer
C	ASUSTeK COMPUTER INC.	RD1_EE1

Date: Monday, July 25, 2016 Sheet 48 of 102

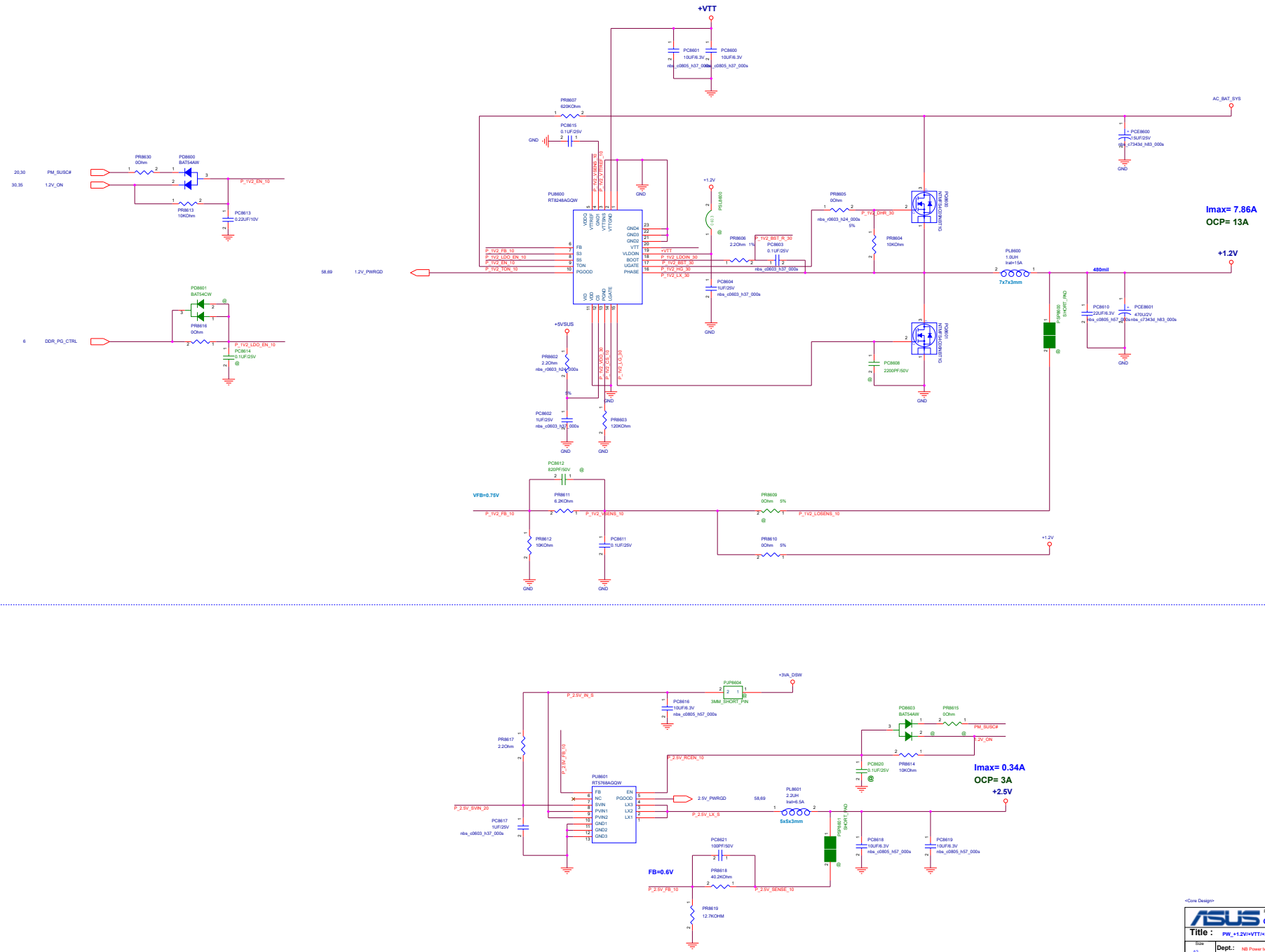
Load Switch

Main Board



Project Name: GL502VM			Rev: 1.0
Title : PW_LOAD SWITCH			
Size: A3	Dept.: NB Power team	Engineer: Edison	
Date: Monday, July 25, 2016	Sheet 88 of 102		

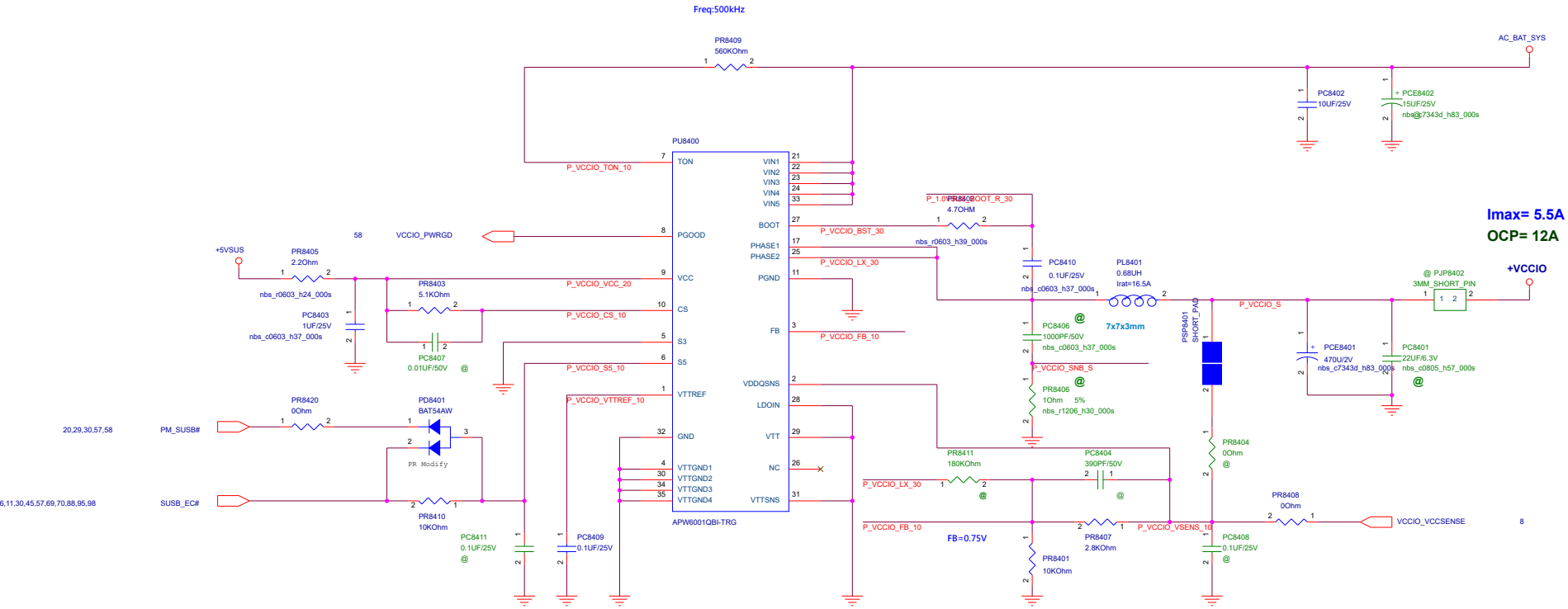
+1.2V / +VTT / +2.5V[For Memory]



<Core Design>

ASUS	Project Name: GL502VM		Rev: 1.0
Title : PW_+1.2V/+VTT/+2.5V			
Size: A2	Dept.: NB Power team	Engineer: Edison	
Date: Monday, July 25, 2016	Sheet: 86 of 102		

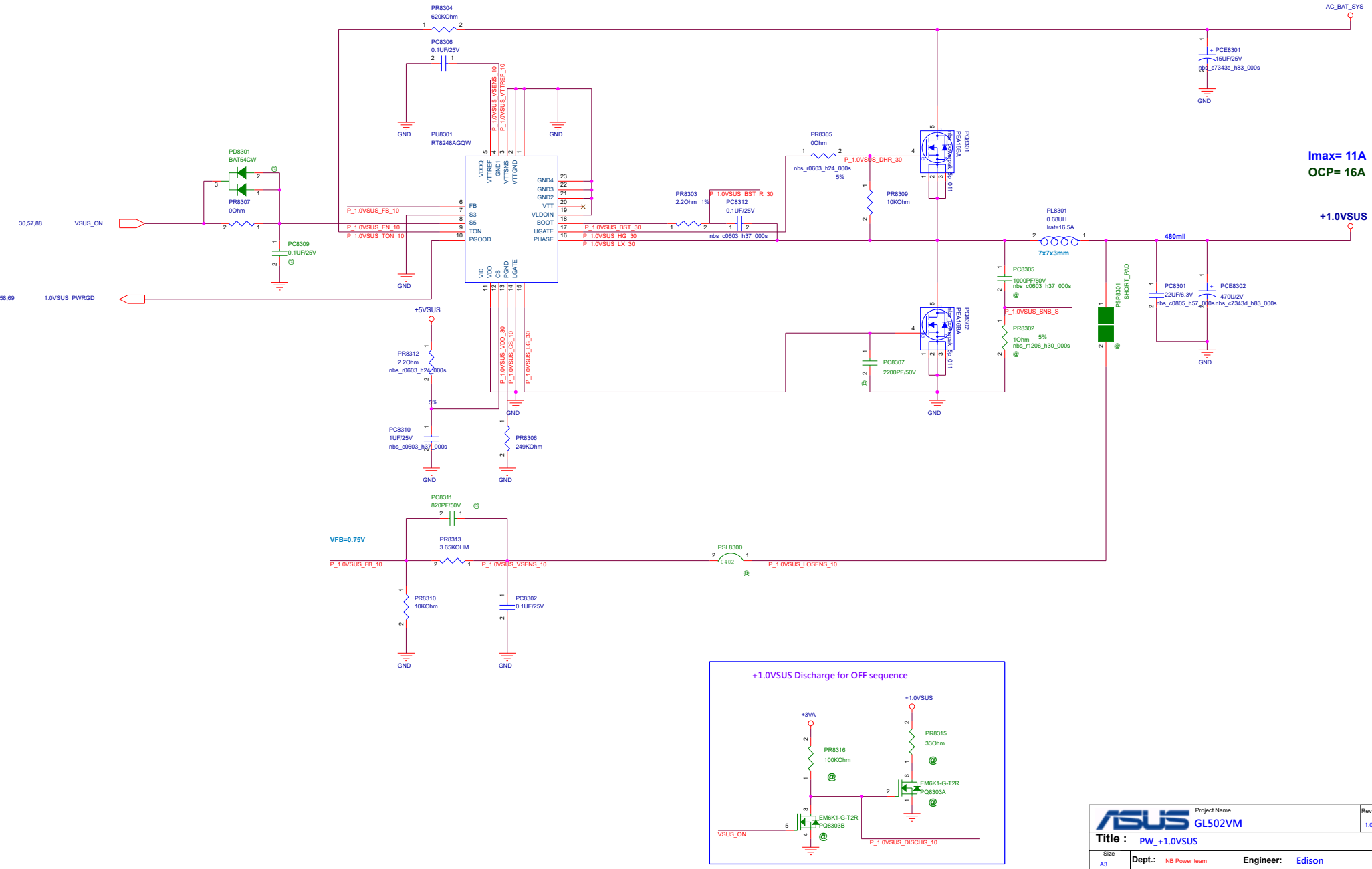
+VCCIO [For CPU]



<Variant Name>

ASUS	Project Name: GL502VM	Rev: 2.0
Title : PW_+VCCIO		
Size: A3	Dept.: NB Power Team	Engineer: Edison
Date: Monday, July 25, 2016	Sheet 84 of 102	

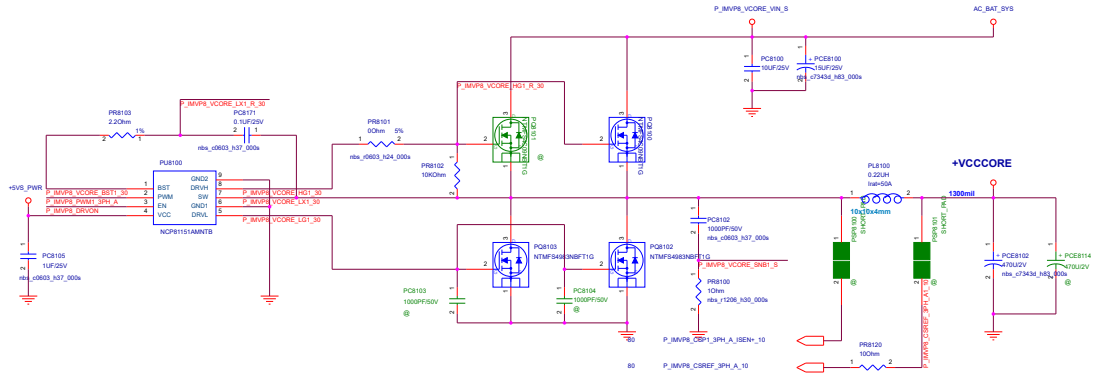
+1.0VSUS [For PCH]

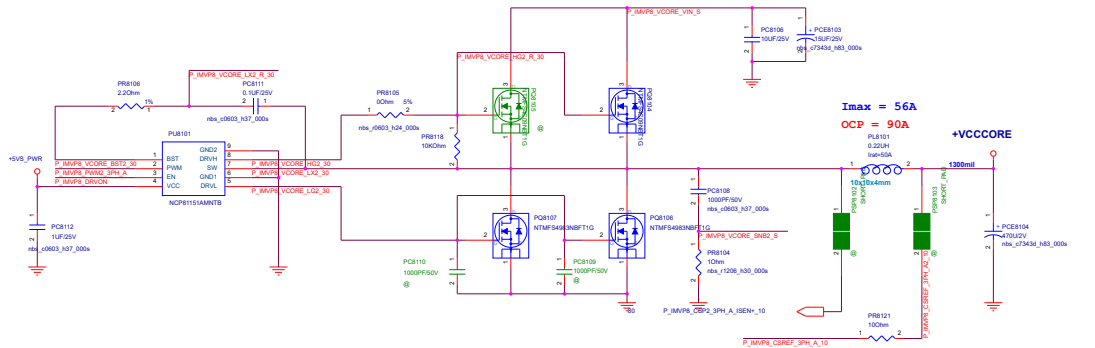


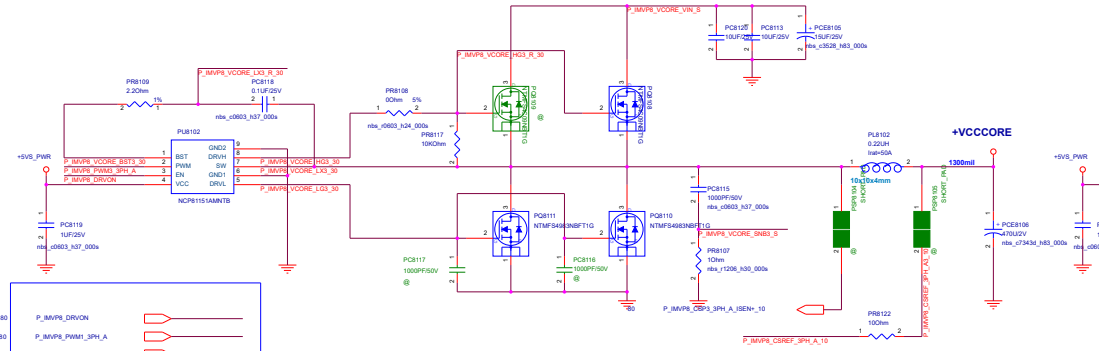
Project Name: GL502VM			Rev: 1.0
Title: PW_+1.0VSUS			
Size: A3	Dept.: NB Power team	Engineer: Edison	
Date: Monday, July 25, 2016	Sheet 83 of 102		

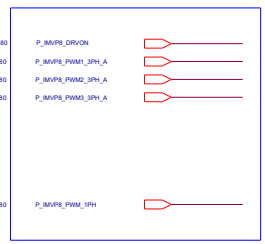
ASUS	Project Name: GL502	Rev: 1.0
Title :	POWER_+VGFX_CORE	
Size: A	Dept.: NB Power team	Engineer: Edison
Date: Monday, July 25, 2016	Sheet 82 of 102	

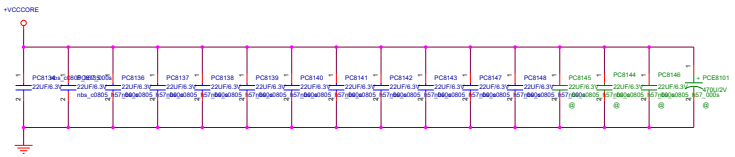
Skylake IMVP8 Power [For CPU]

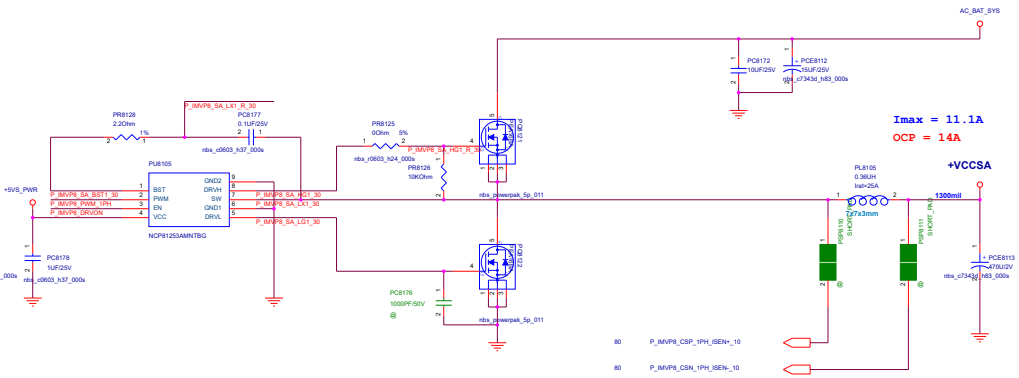


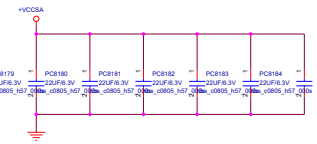






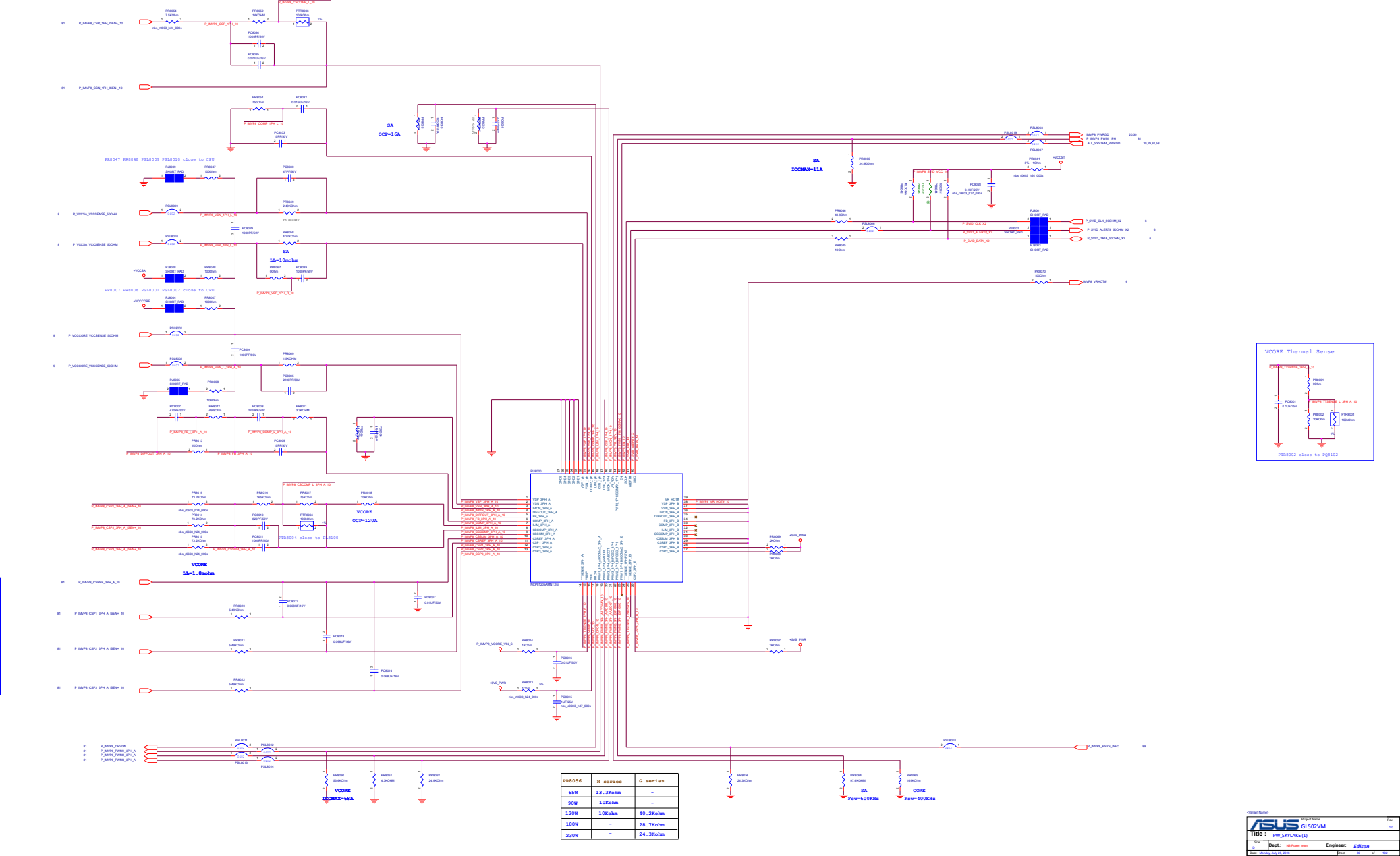






<variant_name>

ASUS	Project Name: GL502VM		Rev: 1.0
Title : PW_SKYLAKE (2)			
Size: A3	Dept.: NB Power team	Engineer: Edison	
Date: Monday, July 25, 2016	Sheet 81 of 102		



PR8056	N series	G series
65W	13.3Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm

Project Name	GL502VM
Rev	1.0
Title :	PW_SKYLAKE (1)
Size	D
Dept.:	NB Power team
Engineer:	Edison
Date:	Monday, July 25, 2016
Sheet	80 of 102

<Variant Name>

OTH_for test only

RD1_EE1

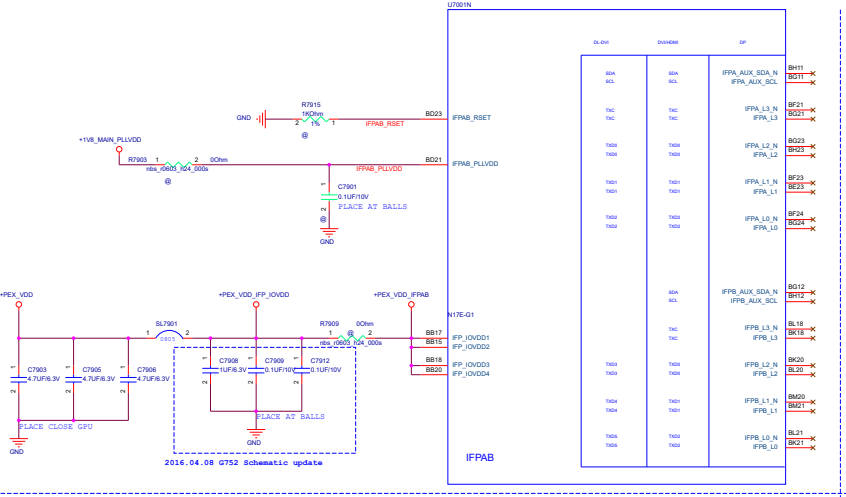
ASUSTeK COMPUTER INC. NB1

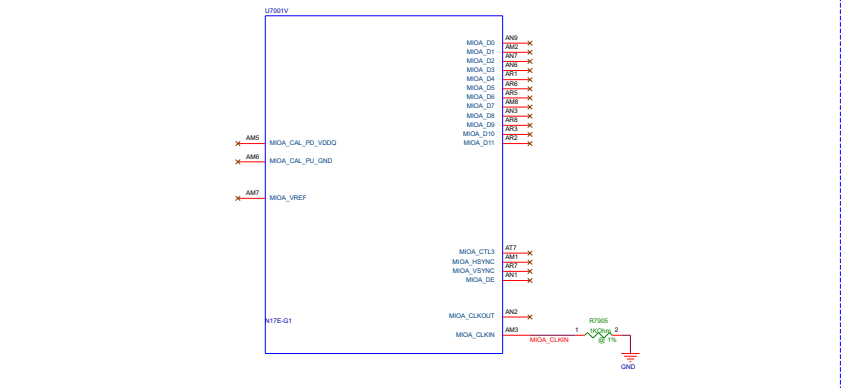
A

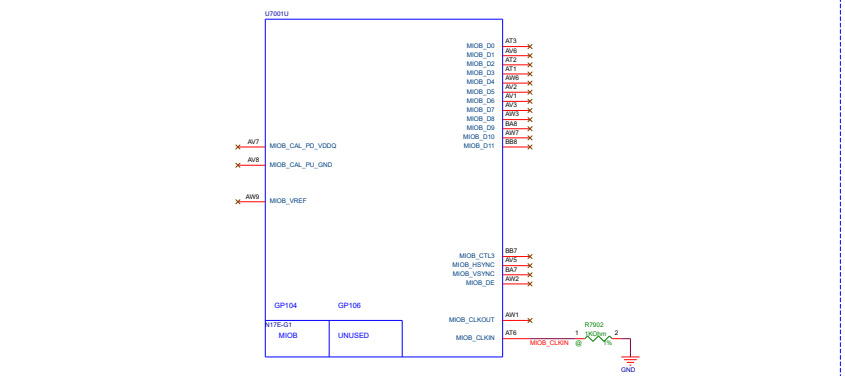
GL502

1.0

Monday, July 25, 2016







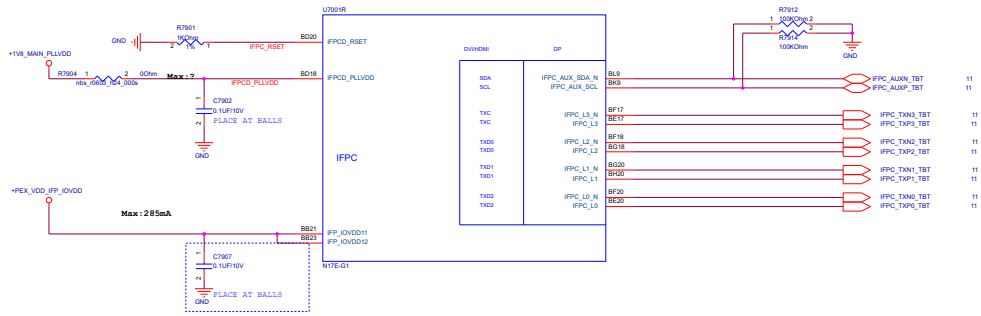
15.2.3 Unconnected Signals (NC)

The following guidelines apply to unused MIO interfaces:

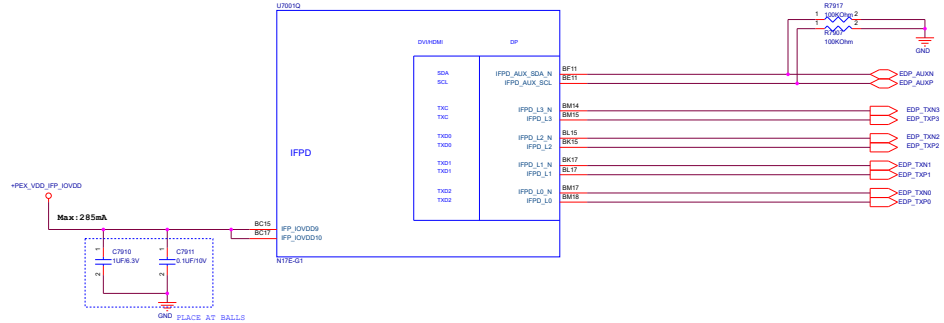
- Power up all VDD18 pins.
- Leave MIO data pins and clock pins floating.

Main Board

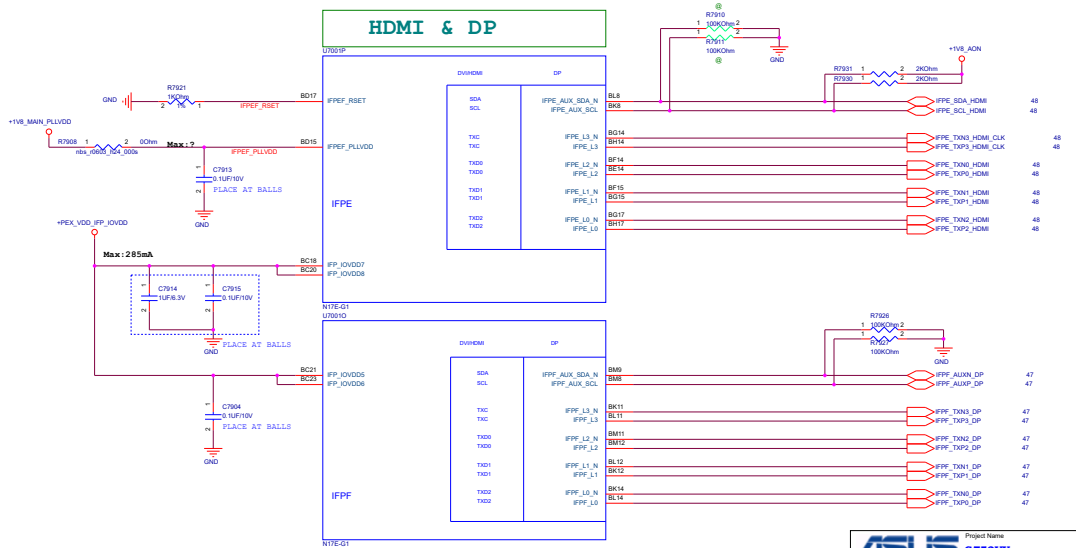
DP(Intel Thunderbolt)



EDP(4Lane Panel)



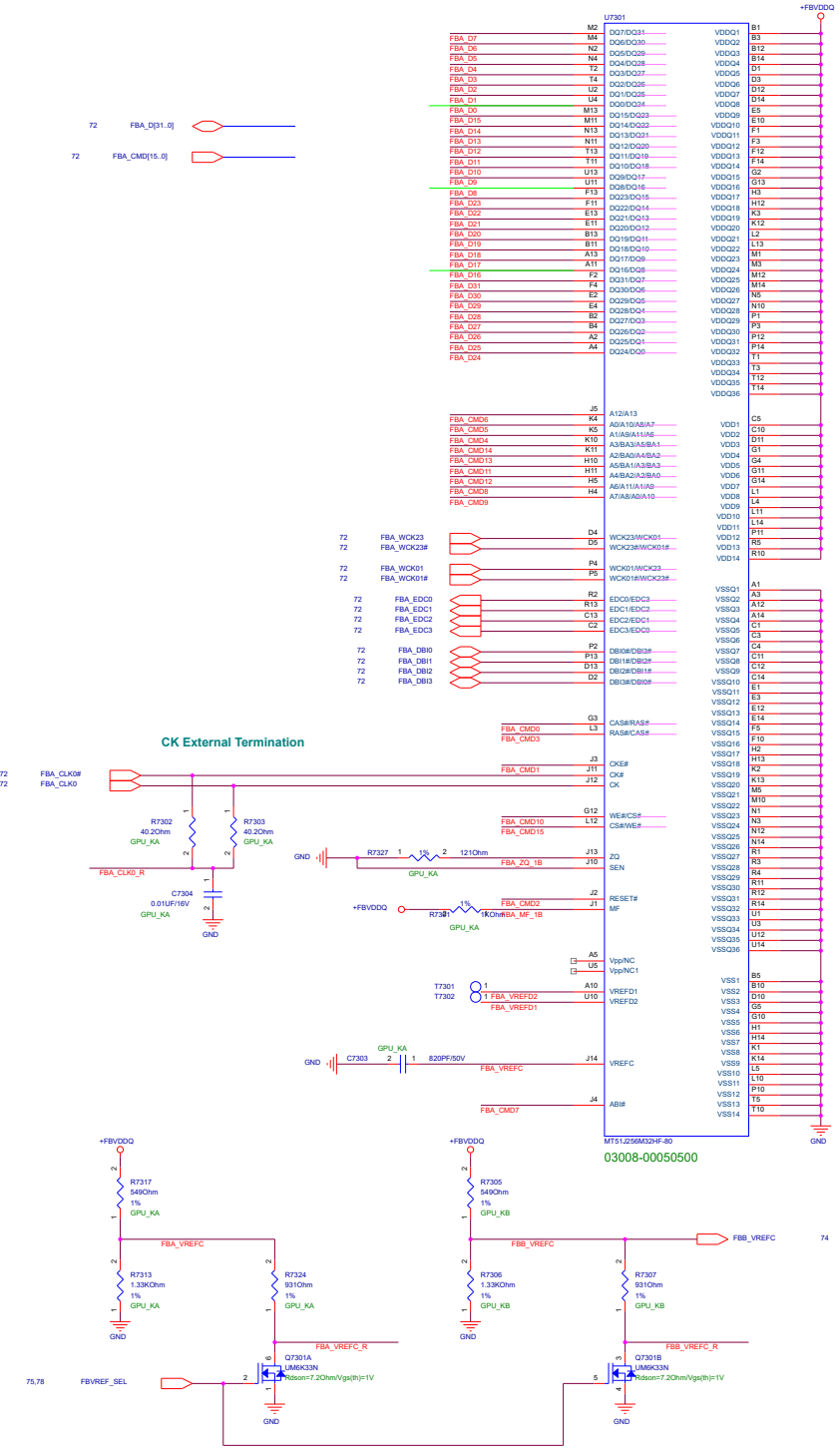
HDMI & DP



Project Name: G752VY			Rev: 2.0
Title: GPU_DP/EDP/HDMI			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: Ashton_yang	
Date: Monday, July 25, 2016	Sheet: 79	of: 102	

FBA Partition Memory (1 of 2)

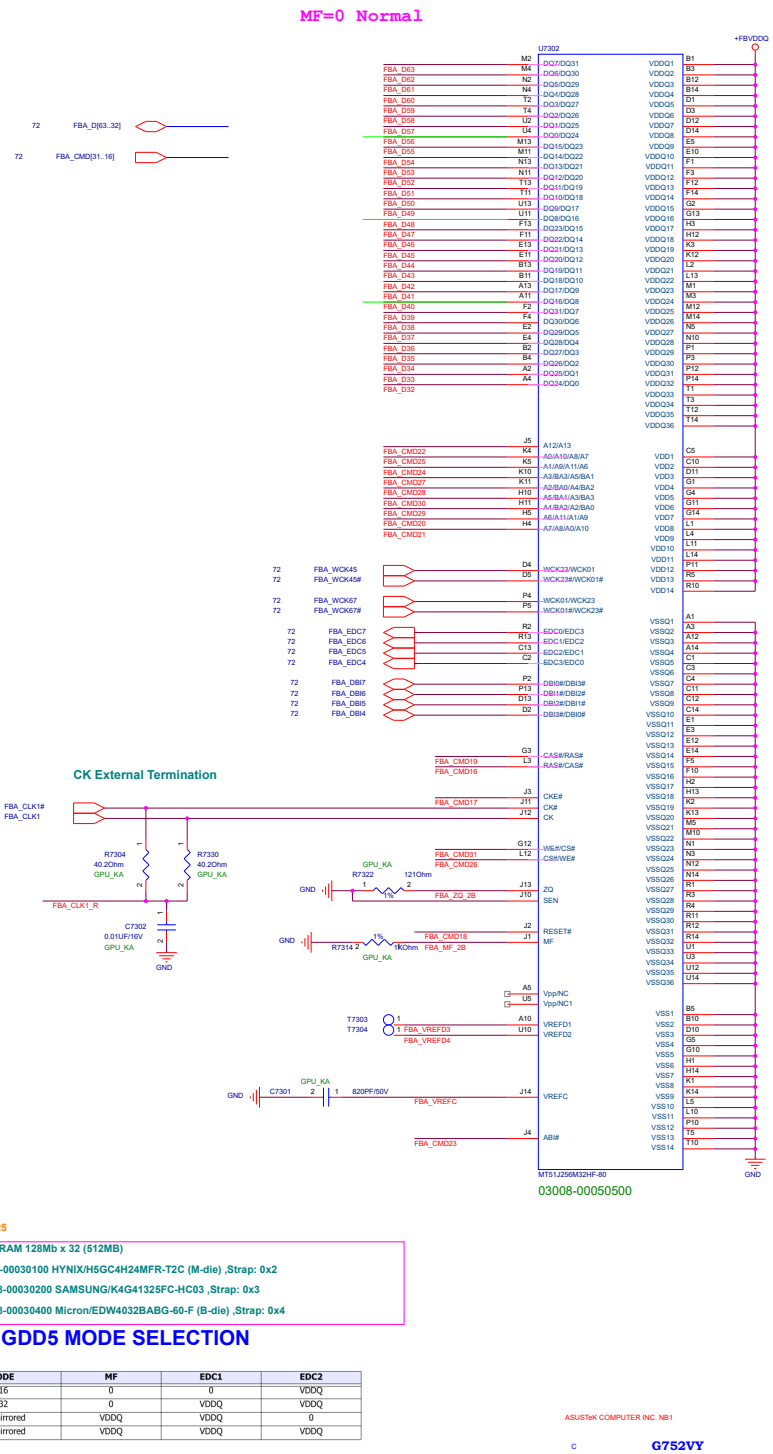
MF=1 Mirror



03008-00050500

FBA Partition Memory (2 of 2)

MF=0 Normal



03008-00050500

R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

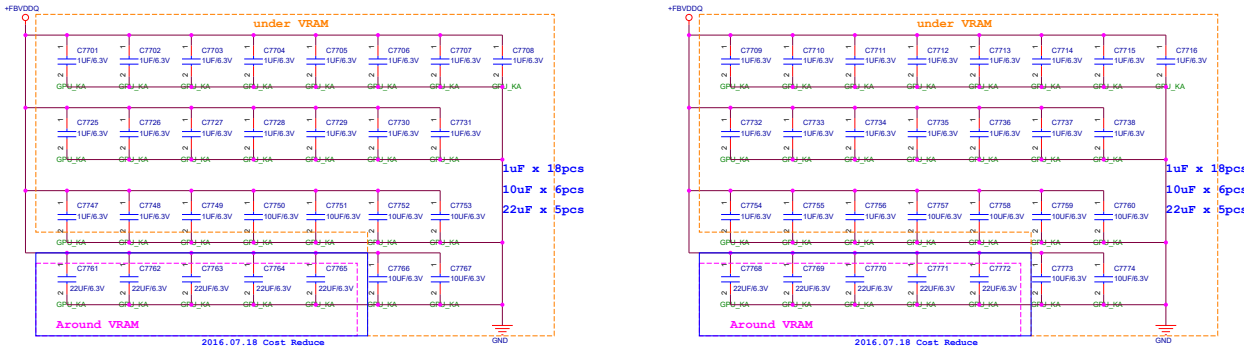
3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

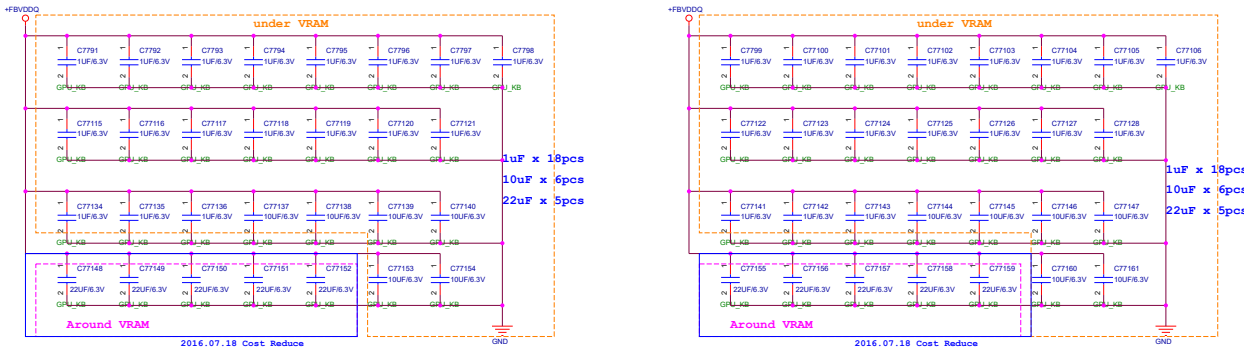
MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

Main Board

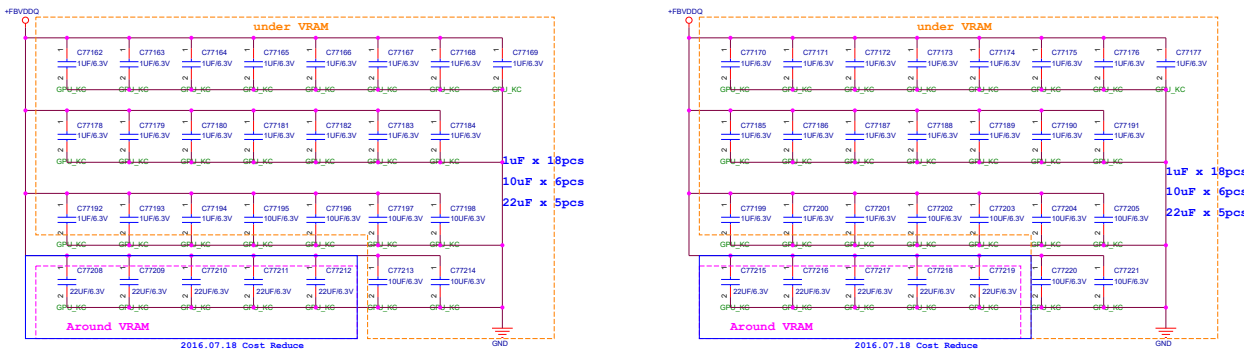
Chanel A



Chanel B

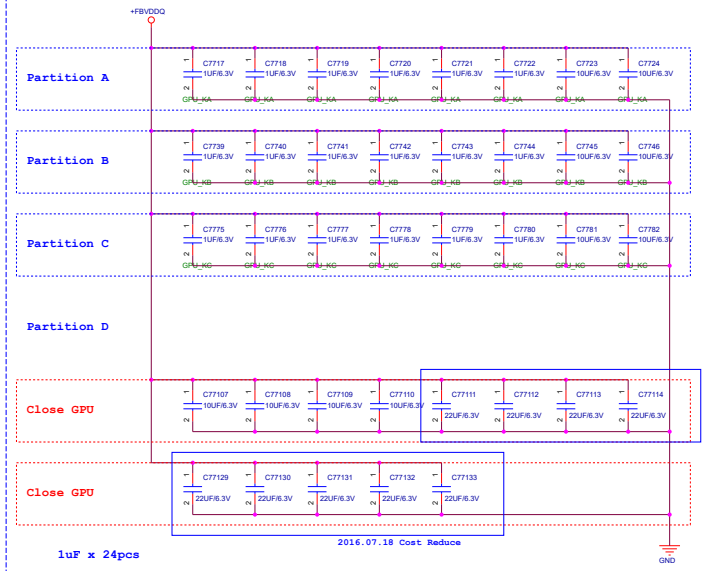


Chanel C

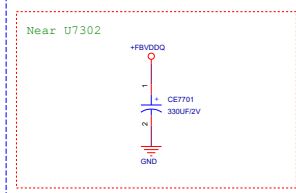


Chanel D

VRAM PWR_FBVDDQ

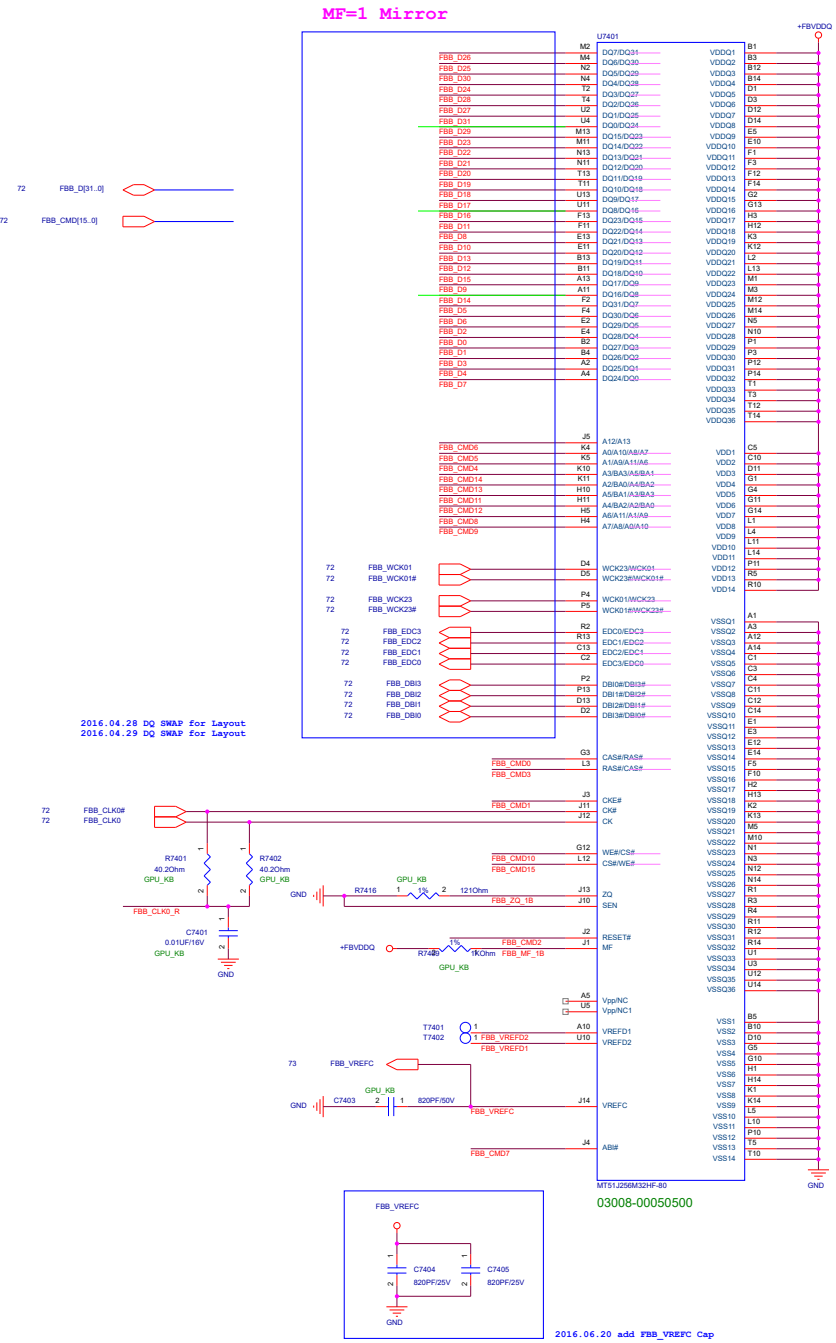


1uF x 24pcs
10uF x 12pcs
22uF x 9pcs



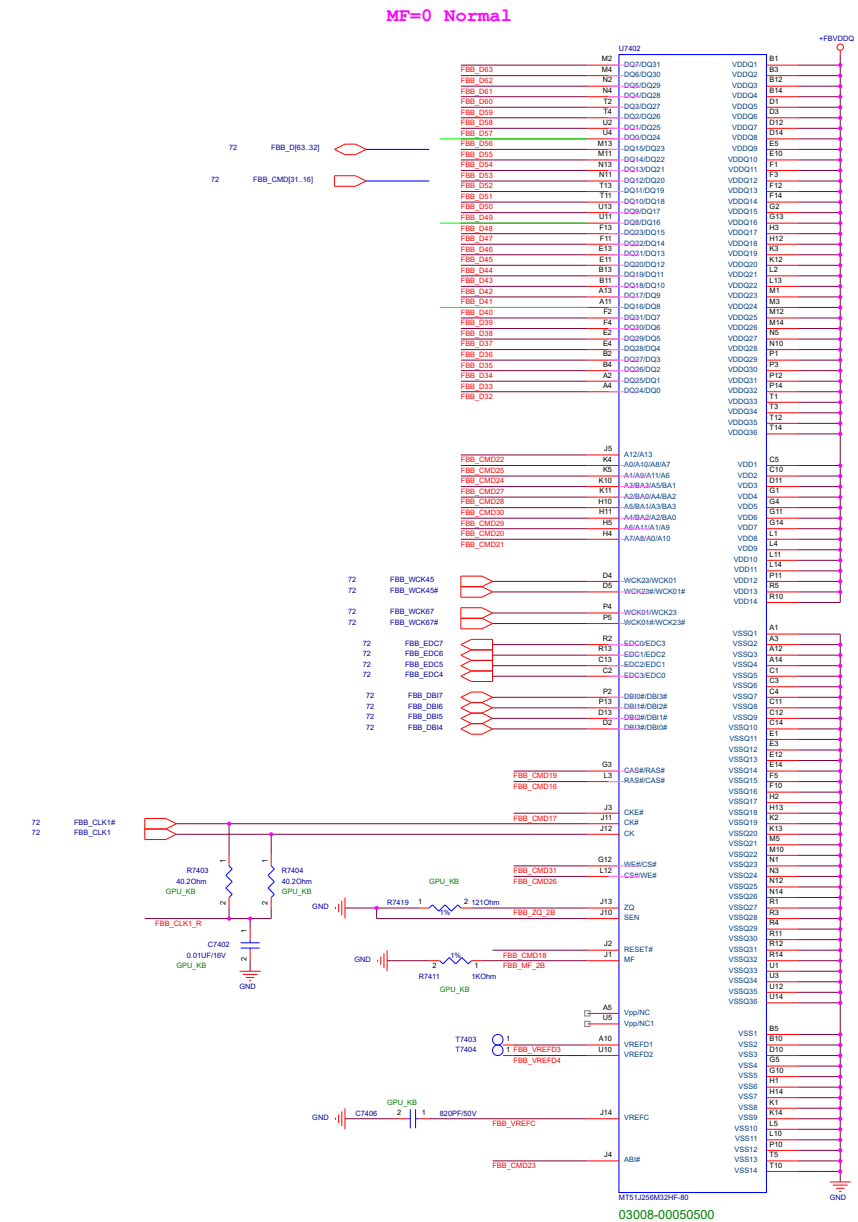
VRAM CAP.

FBB Partition Memory (1 of 2)



03008-00050500

FBB Partition Memory (2 of 2)



03008-00050500

R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

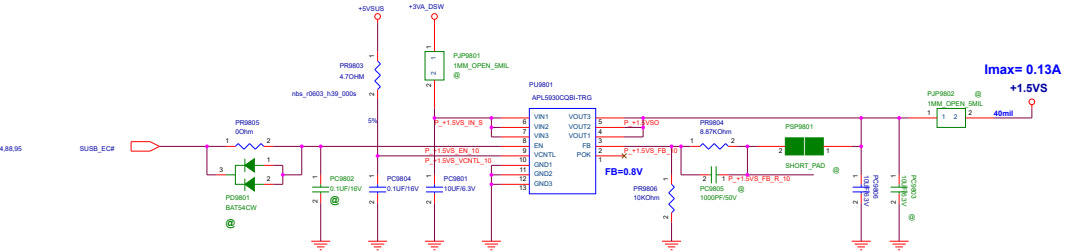
MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

VRAM-CHANNEL B

Ashton_yang

ASUS	Project Name: G752VY	Rev: 2.0
Title : VRAM-CHANNEL D		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ashton_yang
Date: Monday, July 25, 2016	Sheet: 76 of 102	

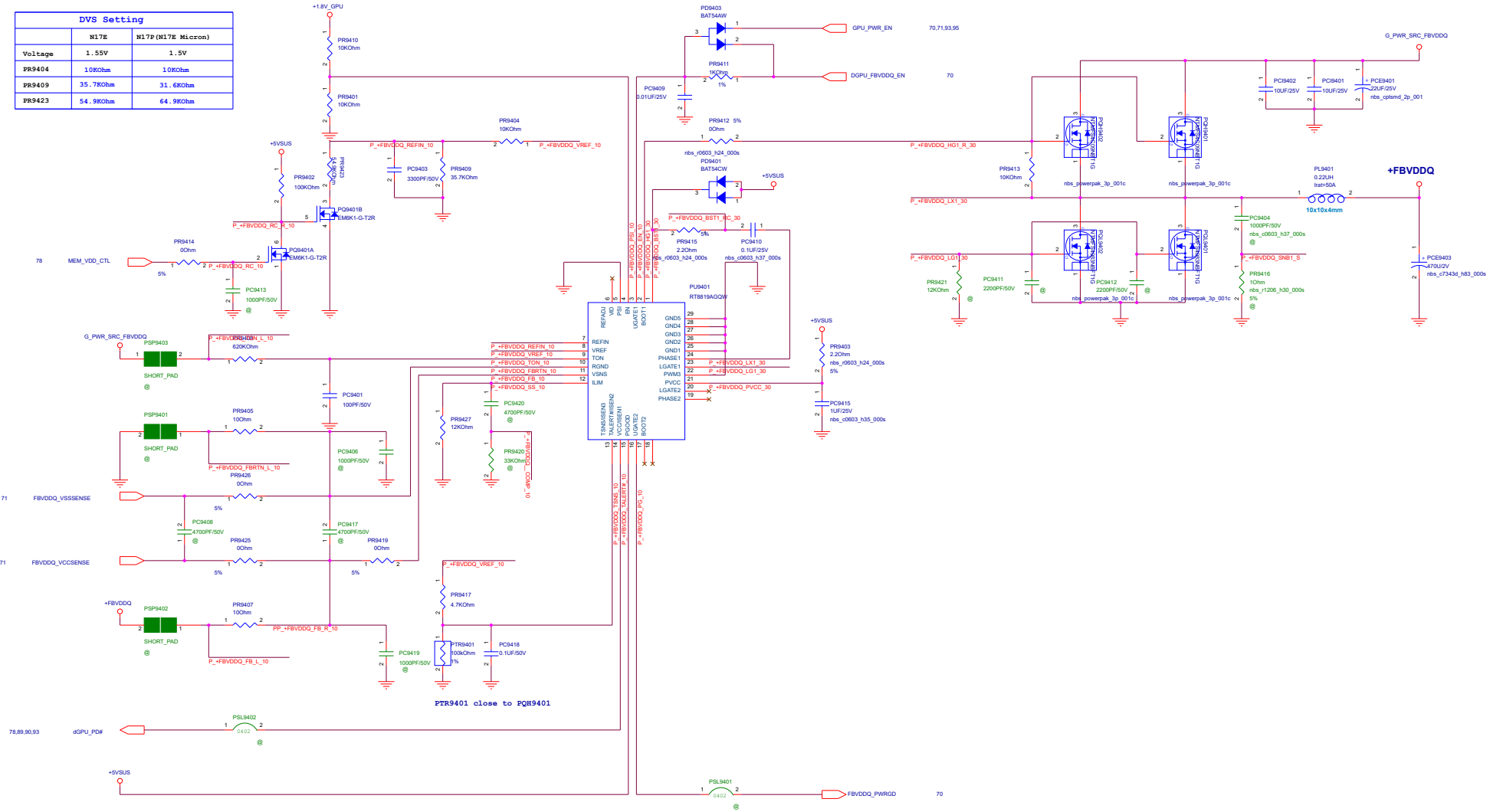
+1.5VS



ASUS	Project Name: GL502VM		Rev: 1.0
Title : POWER_+V1.5VS			
Size: A4	Dept.: NB Power team	Engineer: Edison	
Date: Monday, July 25, 2016	Sheet 98 of 102		

+FBVDDQ [For VRAM]

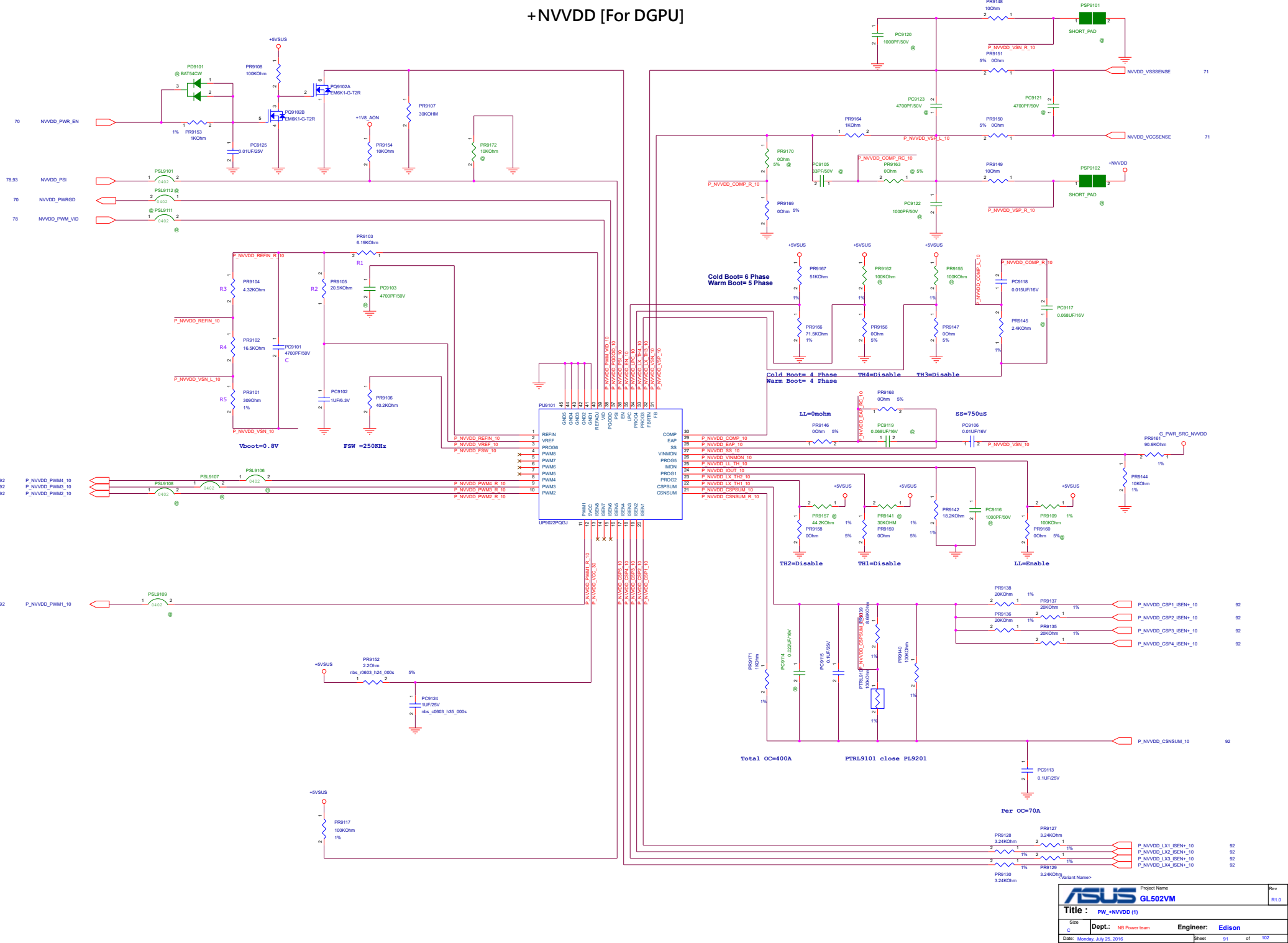
DVS Setting		
	N17E	N17P(N17E Micron)
Voltage	1.55V	1.5V
PR9404	10KOhm	10KOhm
PR9409	35.7KOhm	31.6KOhm
PR9423	54.9KOhm	64.9KOhm



<Variant Name>

ASUS	Project Name: GL502VM		Rev: R1.0
Title : PW_+FBVDDQ			
Size: C	Dept.: NB Power Team	Engineer: Edison	
Date: Monday, July 25, 2016	Sheet 94 of 102		

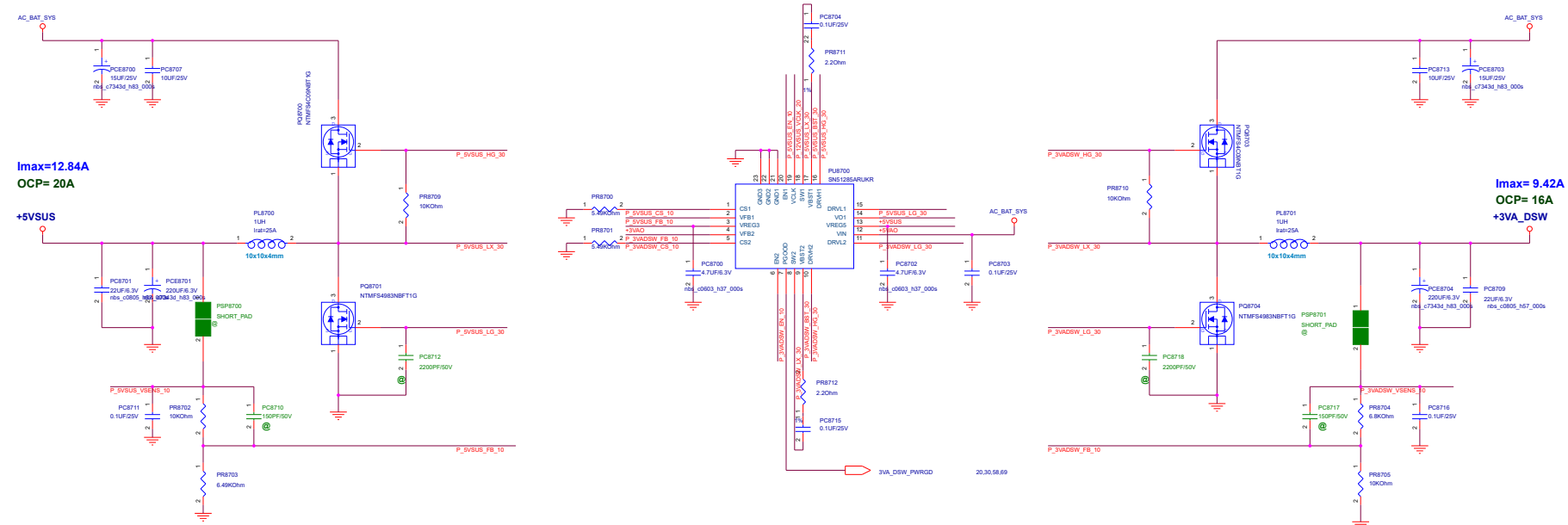
+NVVDD [For DGPU]

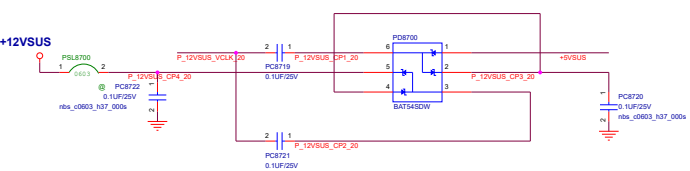


Project Name	GL502VM
Rev	R1.0
Title :	PW_+NVVDD (1)
Size	C
Dept.:	NB Power team
Engineer:	Edison
Date:	Monday, July 25, 2016
Sheet	91 of 102

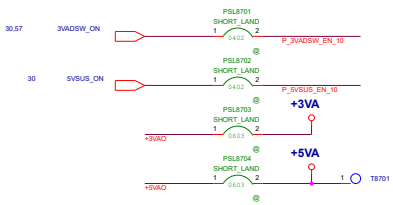
<Variant Name>

+3VA_DSW / +5VSUS [System Power]





請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

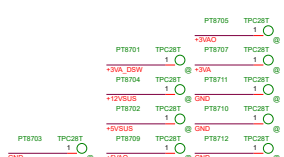


Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0



Project Name

GL502

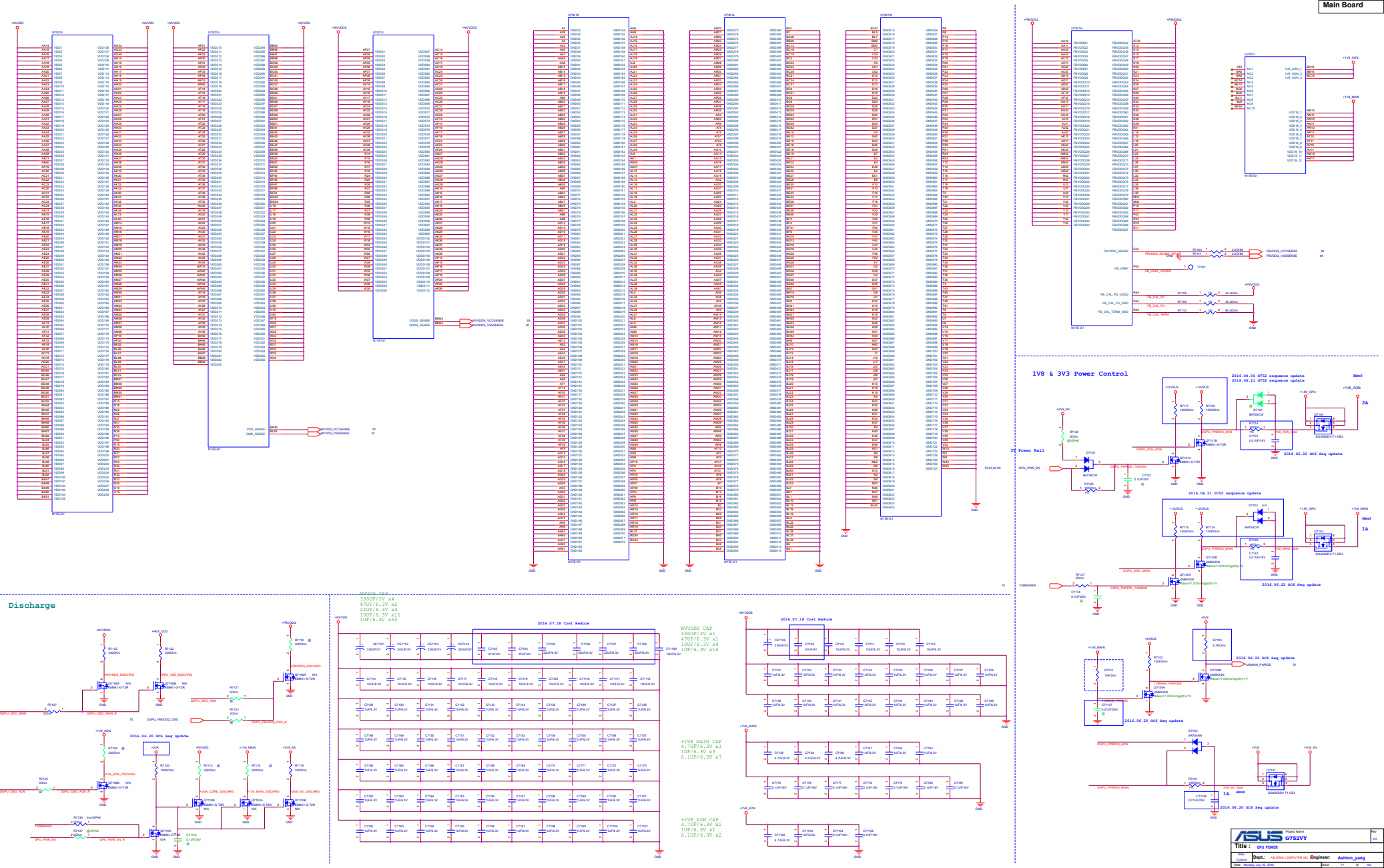
Rev

1.0

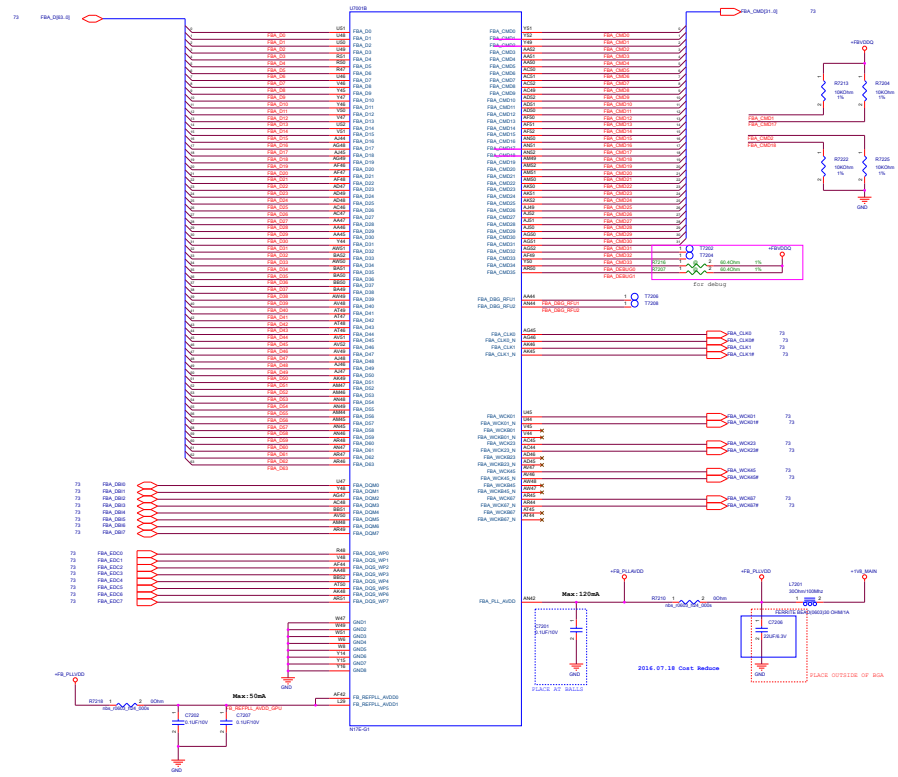
Title : POWER_+VGFX_CORE

Size	Dept.:	Engineer:
A	NB Power team	Edison

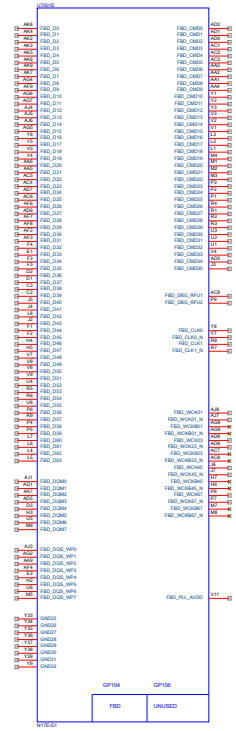
Date: Monday, July 25, 2016


Main Board
1V8 & 3V3 Power Control
2014.04.04 0752 sequence update
2014.04.21 0752 sequence update
2014.06.22 0C6 Seq update
2014.06.21 0752 sequence update
2014.06.20 0C6 Seq update
Discharge
NVVDDS CAP
330UF/2V x4
470UF/6.3V x2
22UF/6.3V x11
10UF/6.3V x50
2014.07.18 Cost Reduce
NVVDDS CAP
330UF/2V x1
470UF/6.3V x1
100UF/6.3V x4
10UF/6.3V x16
+1V8_MAIN CAP
4.7UF/6.3V x3
10UF/6.3V x3
0.10UF/6.3V x7
+1V8_AON CAP
4.7UF/6.3V x1
10UF/6.3V x1
0.10UF/6.3V x2
Project Name
G752VY
Rev
1.0
Title :
GPU_POWER
Size
Custom
Dept.:
ASUSTeK COMPUTER INC.
Engineer:
Ashton_yang
Date:
Monday, July 28, 2014
Sheet
71
of
102

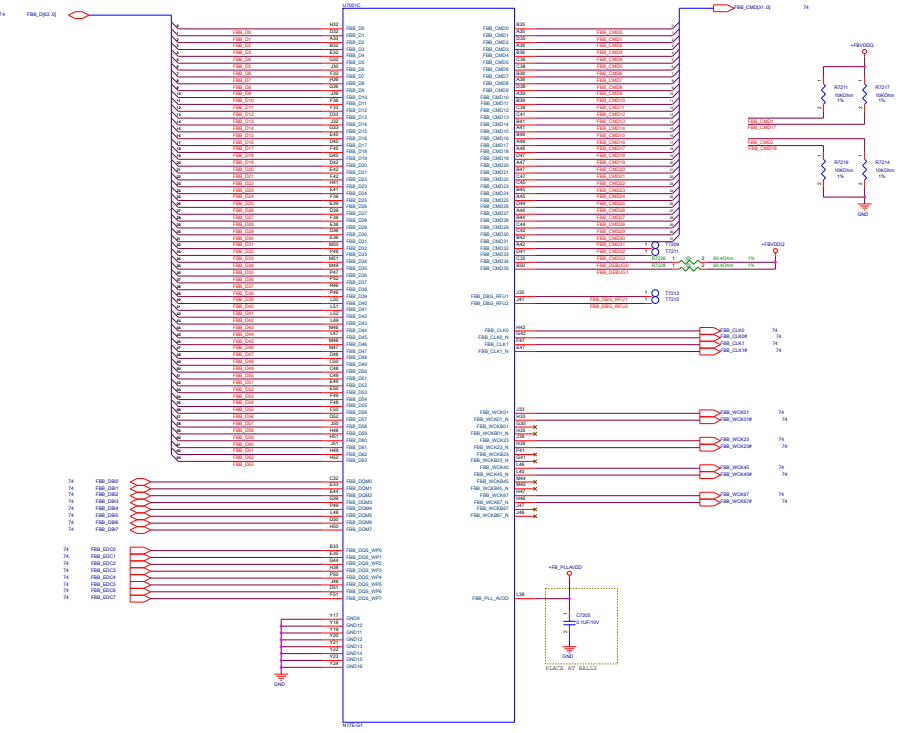
MEMORY: GPU FB Partition A



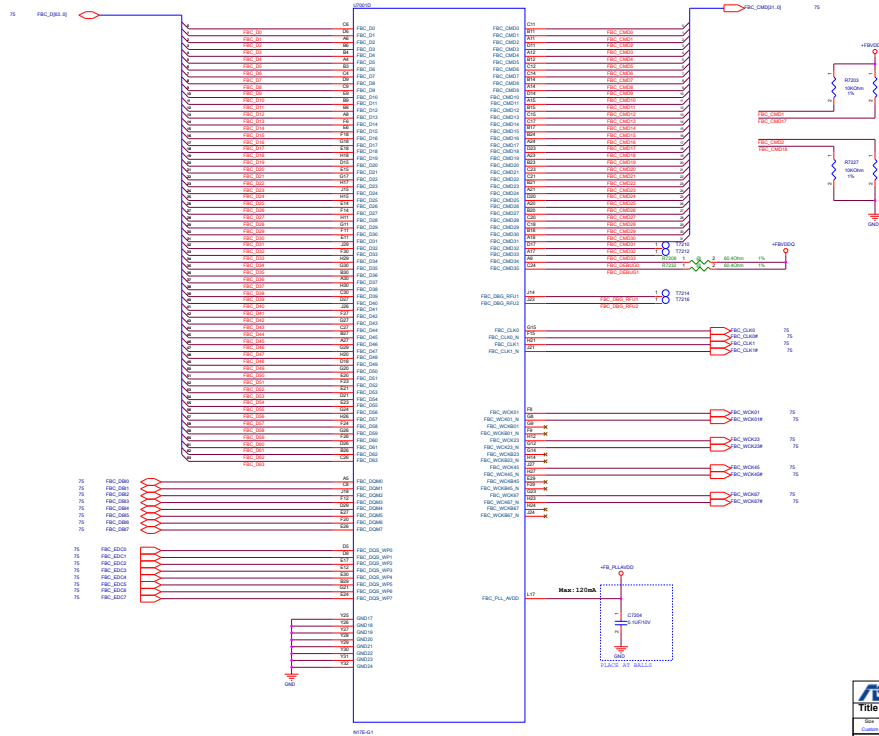
MEMORY: GPU FB Partition D



MEMORY: GPU FB Partition B



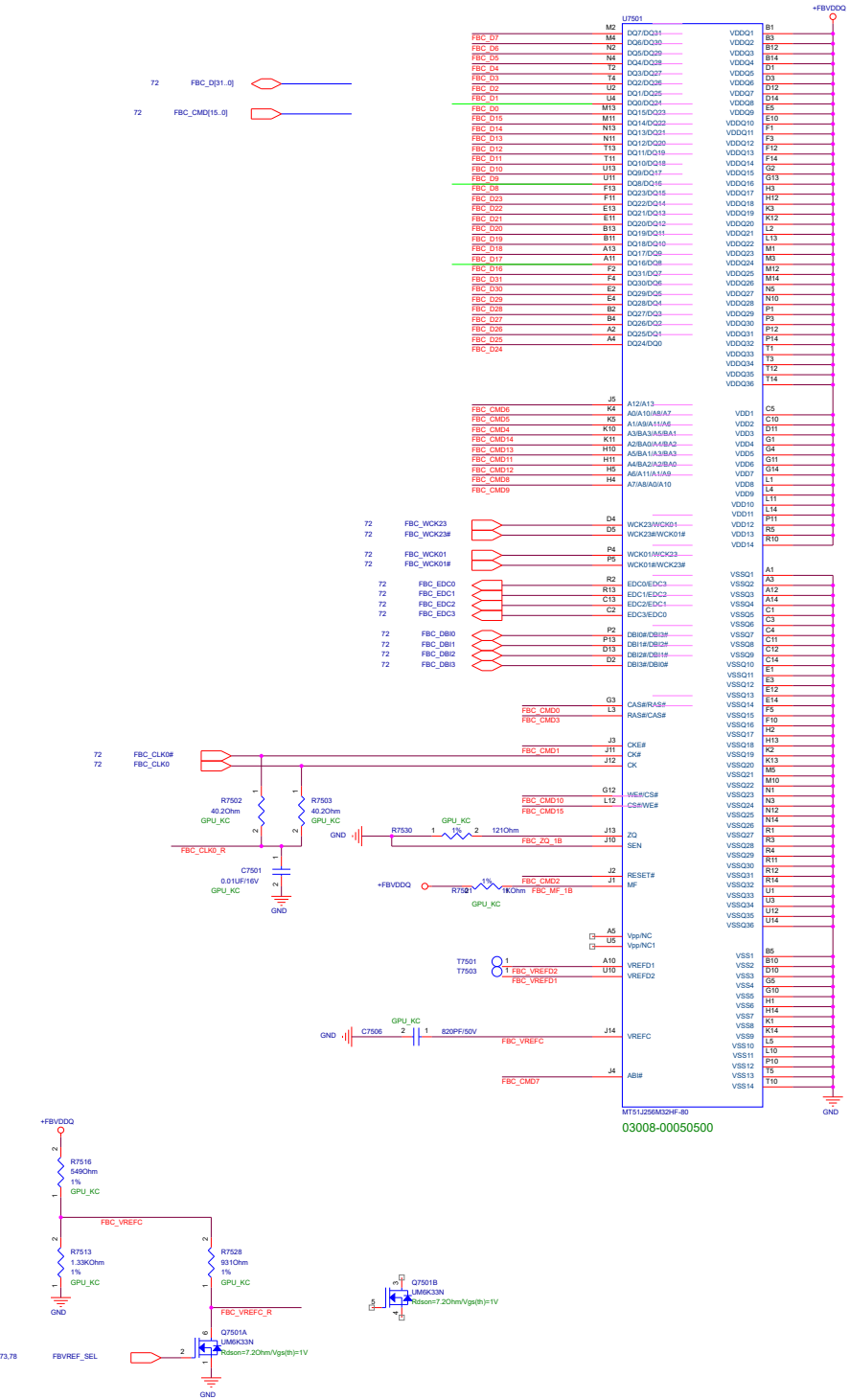
MEMORY: GPU FB Partition C



ASUS	Project Name: G752VY		Rev: 2.0
Title :	GPU_FRAME BUFFER		
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: Ashton_yang	
Date: Monday, July 25, 2016		Sheet: 72 of 102	

FBC Partition Memory (1 of 2)

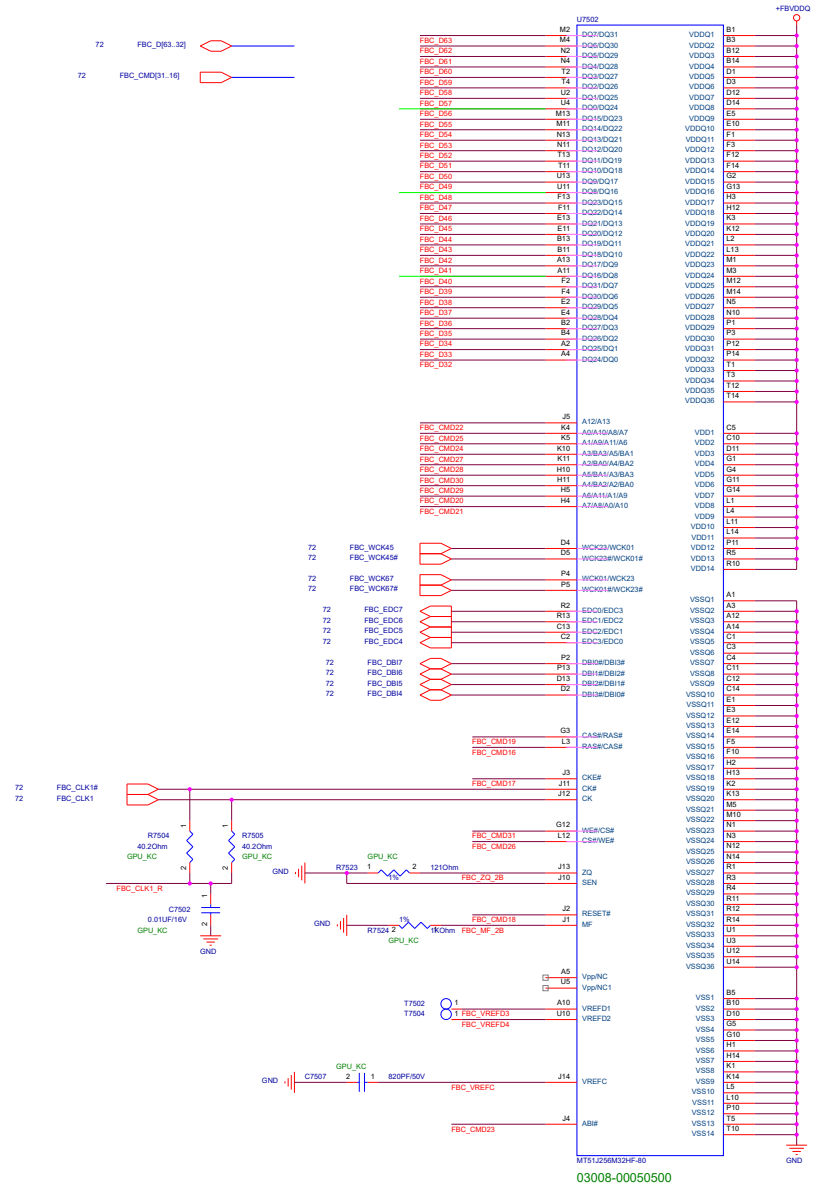
MF=1 Mirror



03008-00050500

FBC Partition Memory (2 of 2)

MF=0 Normal



03008-00050500

R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

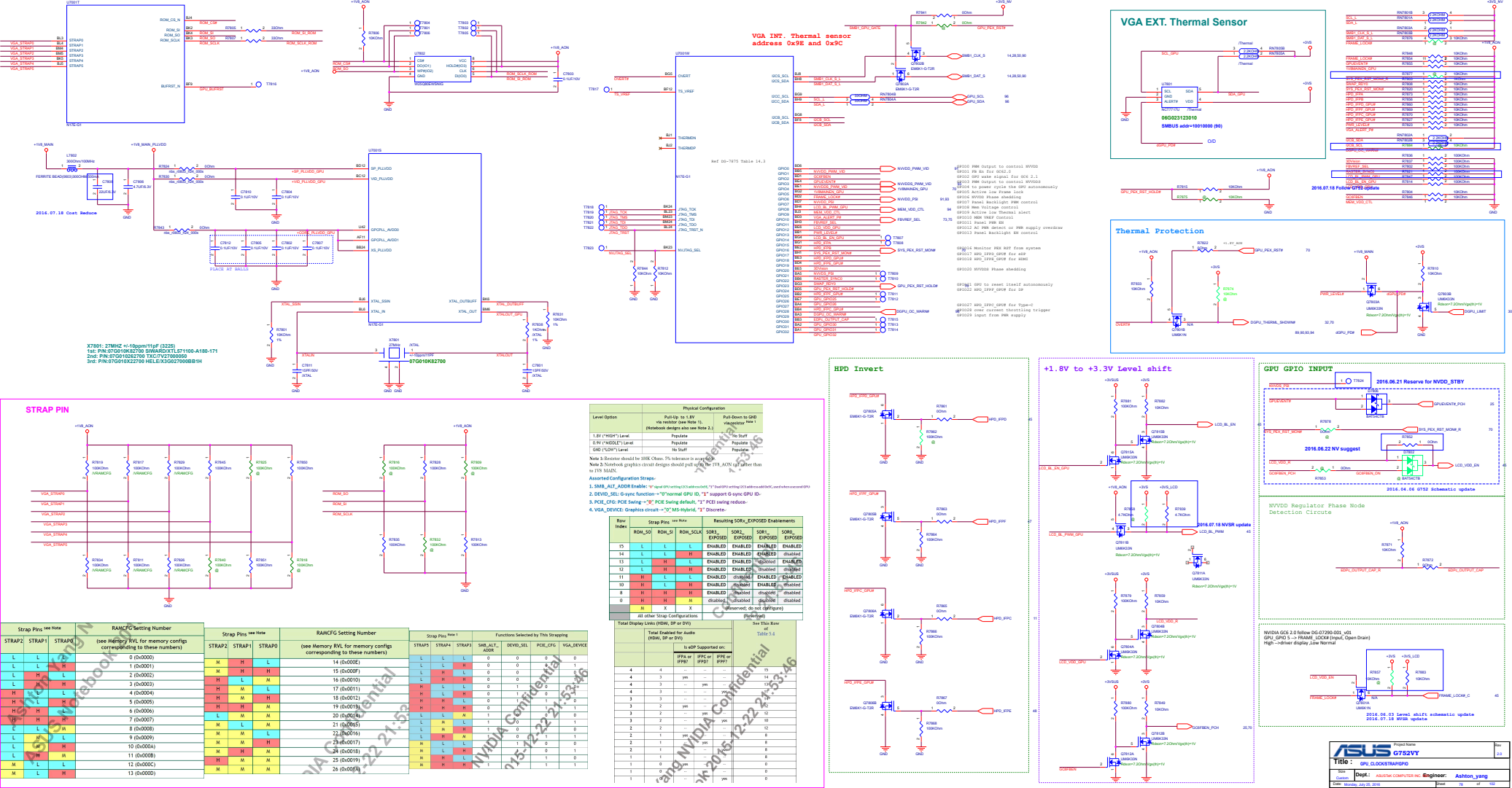
2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

ASUS	Project Name: G752VY		Rev: 2.0
Title :	VRAM-CHANNEL C		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ashton_yang	
Date: Monday, July 25, 2016	Sheet 75 of 102		


VGA INT. Thermal sensor address 0x9E and 0x9C
VGA EXT. Thermal Sensor
SMBUS addr=10010000 (90)
06G023123010
Thermal Protection
2016.07.18 Cost Reduce
2016.07.18 Follow G792 update
X7801: 27MHZ +/-10ppm/11pF (3225)
1st: P/N:07G0100K82700 SIWARD/XTL571100-A180-171
2nd: P/N:07G0102Z2700 TXC/7V27000050
3rd: P/N:07G010X22700 HELE/X3G027000B31H
07G010K82700
STRAP PIN
HPD Invert
+1.8V to +3.3V Level shift
GPU GPIO INPUT
2016.06.21 Reserve for NVDD_STBY
2016.06.22 NV suggest
2016.04.06 G752 Schematic update
NVVDD Regulator Phase Node Detection Circute
2016.07.18 NVSR update
NVIDIA G75 2.0 follow DG-07290-001 v01
GPU_GPIO 5 --> FRAME_LOCKH (input, Open Drain)
High -->driver display_Low Normal
2016.06.03 Level shift schematic update
2016.07.18 NVSR update
ASUS
Project Name: G752VY
Title : GPU_CLOCK/STRAP/GPIO
Size: Custom
Dept.: ASUSTeK COMPUTER INC.
Engineer: Ashton_yang
Date: Monday, July 25, 2016
Sheet 75 of 102
Rev: 2.0
Strap Pins (see Note) | RAMCFG Setting Number
STRAP2 | STRAP1 | STRAP0 | (see Memory RVL for memory configs corresponding to these numbers)
L | L | L | 0 (0x0000)
L | L | H | 1 (0x0001)
L | H | L | 2 (0x0002)
L | H | H | 3 (0x0003)
H | L | L | 4 (0x0004)
H | L | H | 5 (0x0005)
H | H | L | 6 (0x0006)
H | H | H | 7 (0x0007)
L | L | M | 8 (0x0008)
L | M | L | 9 (0x0009)
L | M | H | 10 (0x000A)
L | H | M | 11 (0x000B)
M | L | L | 12 (0x000C)
M | L | H | 13 (0x000D)
M | H | L | 14 (0x000E)
M | H | H | 15 (0x000F)
H | L | M | 16 (0x0010)
H | M | L | 17 (0x0011)
H | M | H | 18 (0x0012)
H | H | M | 19 (0x0013)
L | M | M | 20 (0x0014)
M | L | M | 21 (0x0015)
M | M | L | 22 (0x0016)
M | M | M | 23 (0x0017)
M | H | M | 24 (0x0018)
H | M | M | 25 (0x0019)
M | M | H | 26 (0x001A)
Strap Pins (Note 1) | Functions Selected by This Strapping
STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE
L | L | L | 0 | 0 | 0 | 0
L | L | H | 0 | 0 | 1 | 1
L | H | L | 0 | 0 | 2 | 2
L | H | H | 0 | 0 | 3 | 3
H | L | L | 0 | 1 | 0 | 4
H | L | H | 0 | 1 | 1 | 5
H | H | L | 0 | 1 | 2 | 6
H | H | H | 0 | 1 | 3 | 7
L | L | M | 1 | 0 | 0 | 8
L | M | L | 1 | 0 | 1 | 9
L | M | H | 1 | 0 | 2 | 10
L | H | M | 1 | 0 | 3 | 11
M | L | L | 1 | 1 | 0 | 12
M | L | H | 1 | 1 | 1 | 13
M | H | L | 1 | 1 | 2 | 14
M | H | H | 1 | 1 | 3 | 15
Level Option | Physical Configuration
Pull-Up to 1.8V via resistor (see Note 1). (Notebook designs also see Note 2.) | Pull-Down to GND via resistor Note 1 | No Stuff
1.8V ("HIGH") Level | Populate | No Stuff
0.9V ("MIDDLE") Level | Populate | Populate
GND ("LOW") Level | No Stuff | Populate
Row Index | Strap Pins See Note | Resulting SORx_EXPOSED Enablements
ROM_SO | ROM_SI | ROM_SCLK | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED
15 | L | L | L | ENABLED | ENABLED | ENABLED | ENABLED
14 | L | L | H | ENABLED | ENABLED | ENABLED | disabled
13 | L | H | L | ENABLED | ENABLED | disabled | ENABLED
12 | L | H | H | ENABLED | ENABLED | disabled | disabled
11 | H | L | L | ENABLED | disabled | ENABLED | ENABLED
10 | H | L | H | ENABLED | disabled | ENABLED | disabled
9 | H | H | L | ENABLED | disabled | disabled | ENABLED
8 | H | H | H | disabled | disabled | disabled | disabled
M | X | X | (Reserved; do not configure)
All other Strap Configurations | (Reserved)
Total Display Links (HDM, DP or DVI) | Total Enabled for Audio (HDM, DP or DVI) | Is eDP Supported on: IFPA or IFPB | IFPC or IFPD | IFPE or IFPF | See This Row of Table 5.4
4 | 4 | .. | .. | .. | 13
4 | 3 | yes | .. | .. | 14
4 | 3 | .. | yes | .. | 15
3 | 3 | .. | .. | yes | 11
3 | 3 | .. | .. | .. | 12
3 | 2 | yes | .. | .. | 12
3 | 2 | .. | yes | .. | 10
2 | 2 | .. | .. | .. | 12
2 | 1 | yes | .. | .. | 8
2 | 1 | .. | yes | .. | 6
2 | 1 | .. | .. | .. | 8
1 | 1 | .. | .. | .. | 8
1 | 0 | yes | .. | .. | 0
1 | 0 | .. | .. | .. | 0
1 | 0 | .. | yes | .. | 0
Strap Pins See Note | RAMCFG Setting Number
STRAP2 | STRAP1 | STRAP0 | (see Memory RVL for memory configs corresponding to these numbers)
M | H | L | 14 (0x000E)
M | H | H | 15 (0x000F)
H | L | M | 16 (0x0010)
H | M | L | 17 (0x0011)
H | M | H | 18 (0x0012)
H | H | M | 19 (0x0013)
L | M | M | 20 (0x0014)
M | L | M | 21 (0x0015)
M | M | L | 22 (0x0016)
M | M | M | 23 (0x0017)
M | H | M | 24 (0x0018)
H | M | M | 25 (0x0019)
M | M | H | 26 (0x001A)
Confidential
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